VME, VME64 and VME64x
General and technical information

The VMEbus, based on the IEEE 1014 and IEC 821 standards, has become an established industrial standard worldwide.
The VME64 represents an extension of the VME family according to ANSI/VITA 1-1994 and permits 64-bit data traffic. The VME64x extends the VME family according to ANSI/VITA 1.1-1997 and is available with the optional 95/133-pin, 2 mm connector J0. VME64 and VME64x use 160-pins connectors. This system is downward-compatible, so that assemblies with 96-pin connectors to DIN 41612 can still be used.

All Hartmann VMEbus boards are based on the HIGH-SPEED DESIGN concept. Low reflection is achieved by means of uniform signal line surge impedance. Shielding of each individual signal line assures minimal coupling and therefore guarantees trouble-free operation even when expanded to the 64-bit mode with the 2e protocol (160 MByte/s).

Termination

In order to prevent interference on signal lines which might result from reflection at open line ends, these lines must be terminated on the VMEbus. ON/IN-board (on the backplane) or OFF-board (external) termination is possible. A distinction is made between passive and active termination. The advantage of active termination is reduced closed-circuit current consumption. Passive termination features better frequency response and a wider temperature range.

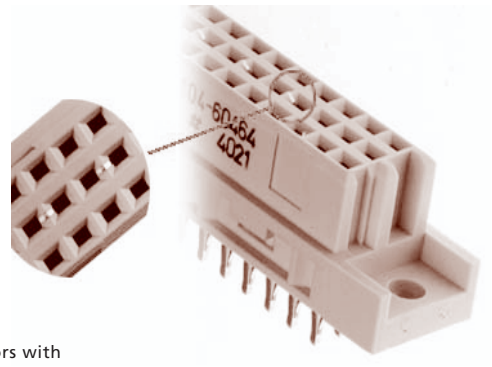
Daisy chain wiring

A distinction is made between manual daisy chaining and automatic daisy chaining.

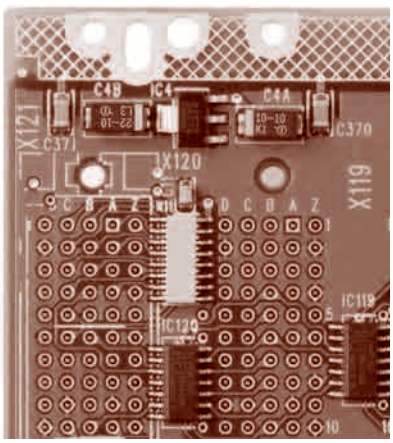
Automatic daisy chaining works without jumpers, i. e. the user does not need to bother with plugging in and removing jumpers. This has the added advantage that incorrect jumper placement due to operator error is precluded.

VME, VME64 and VME64x
General and technical information

Manual daisy chaining



Automatic Daisy Chain with Connectors with Switching Function



Automatic Daisy Chain using the OR logic integrated

Manual daisy chaining:
The daisy chain lines are brought out as gold-plated pins next to the DIN connectors. The jumpers can be inserted on the 0.6 x 0.6 mm pins from the wiring or component side.

Automatic daisy chaining:
Automatic daisy chaining can be implemented in two ways:

- Thanks to the use of connectors with integrated mechanical switches, the contact is automatically opened when a daughter board is inserted and closed when the board is removed.
- The second type of automatic daisy chaining is implemented using the OR logic integrated in the backplane. This logic closes the daisy chain when the daughter board is removed.

VME, VME64 and VME64x
General and technical information

CHASSIS GND connection

There is a solid electrically conductive chassis GND surface in the backplane-to-card rack mounting area. This guarantees EMC-tight mounting of the bus board on the card rack.

HF coupling of card rack and system ground is implemented for VME64 and VME64x by capacitors (10 nF, 200 V in each slot).
Static charges are discharged via a resistor (≥ 1 MΩ).
A combination element (M4 screw and Faston 2.8 or 6.3 x 0.8 mm) is provided for the chassis ground connection.

Power connections

The main operating voltage of is supplied via terminal bars with M6 screw connections for VME64 and VME64x.
The main operating voltages are supplied via dual Fastons with an additional M4 thread for the VMEbus. Optimal daughter board supply and trouble-free operation are ensured by the arrangement of the feed modules on the backplane.

Utility connector

The special signals to the power supply unit and external LEDs are brought out to a separate connector on the backplanes.
Depending on the backplane type, a 7-pin, a 10-pin or a 14-pin connector with a contact spacing of 2.54 mm is used.

Pin Assign. 7-pins Utility connector

Pin	1	2	3	4	5	6	7
	GND Sense	+5 V Sense	GND	+5 V	ACFAIL-	SYSFAIL-	SYSRESET-

Pin Assign. 10-pins Utility connector

Pin	1	2	3	4	5	6	7	8	9	10
	GND	GND Sense	+5 V	+5 V Sense	ACFAIL-	ACFAIL-	SYSFAIL-	SYSFAIL-	SYSRESET-	SYSRESET-

Pin Assign. 14-pins Utility connector

1	2	3	4	5	6	7	8	9	10	11	12	13	14
GND	GND Sense (5 V)	+5 V	+5 V Sense	ACFAIL-	ACFAIL-	SYSFAIL-	SYSFAIL-	SYSRESET-	SYSRESET-	+3.3 V	+3.3 V Sense	GND	GND Sense (3.3 V)

VME, VME64 and VME64x Pin Assignments

Pin Assignments - Geographical Address (VME64x)

Slot Number	GAP* Pin J1-D9	GA4* Pin J1-D17	GA3* Pin J1-D15	GA2* Pin J1-D13	GA1* Pin J1-D11	GA0* Pin J1-D10
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
10	GND	Open	GND	Open	GND	Open
11	Open	Open	GND	Open	GND	GND
12	GND	Open	GND	GND	Open	Open
13	Open	Open	GND	GND	Open	GND
14	Open	Open	GND	GND	GND	Open
15	GND	Open	GND	GND	GND	GND
16	Open	GND	Open	Open	Open	Open
17	GND	GND	Open	Open	Open	GND
18	GND	GND	Open	Open	GND	Open
19	Open	GND	Open	Open	GND	GND
20	GND	GND	Open	GND	Open	Open
21	Open	GND	Open	GND	Open	GND

Pin Assignments J0

Pin	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
2	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
3	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
4	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
5	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
6	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
7	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
8	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
9	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
10	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
11	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
12	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
13	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
14	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
15	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
16	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
17	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
18	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND
19	GND	User Defined	User Defined	User Defined	User Defined	User Defined	GND

VME, VME64 and VME64x
General and technical information

Pin Assignments J1

Pin	ROW Z		ROW A VME	ROW B VME	ROW C VME	ROW D	
	VME64x	VME64				VME64	VME64x
1	MPR	Reserved	D00	BBSY*	D08	Reserved	VPC
2	GND	GND	D01	BCLR*	D09	Reserved	GND
3	MCLK	Reserved	D02	ACFAIL*	D10	Reserved	+V1
4	GND	GND	D03	BG0IN*	D11	Reserved	+V2
5	MSD	Reserved	D04	BG0OUT*	D12	Reserved	RsvU-1
6	GND	GND	D05	BG1IN*	D13	Reserved	-V1
7	MMD	Reserved	D06	BG1OUT*	D14	Reserved	-V2
8	GND	GND	D07	BG2IN*	D15	Reserved	RsvU-2
9	MCTL	Reserved	GND	BG2OUT*	GND	Reserved	GAP*
10	GND	GND	SYSCLK	BG3IN*	SYSFAIL*	Reserved	GA0*
11	RTRY1*	Reserved	GND	BG3OUT*	BERR*	Reserved	GA1*
12	GND	GND	DS1*	BR0*	SYSRESET*	Reserved	+3.3 V
13	RsvBus1	Reserved	DS0*	BR1*	LWORD*	Reserved	GA2*
14	GND	GND	WRITE*	BR2*	AM5	Reserved	+3.3 V
15	RsvBus2	Reserved	GND	BR3*	A23	Reserved	GA3*
16	GND	GND	DTACK*	AM0	A22	Reserved	+3.3 V
17	RsvBus3	Reserved	GND	AM1	A21	Reserved	GA4*
18	GND	GND	AS*	AM2	A20	Reserved	+3.3 V
19	RsvBus4	Reserved	GND	AM3	A19	Reserved	RsvBus5
20	GND	GND	IACK*	GND	A18	Reserved	+3.3 V
21	RsvBus6	Reserved	IACKIN*	SERCLK	A17	Reserved	RsvBus7
22	GND	GND	IACKOUT*	SERDAT*	A16	Reserved	+3.3 V
23	RsvBus8	Reserved	AM4	GND	A15	Reserved	RsvBus9
24	GND	GND	A07	IRQ7*	A14	Reserved	+3.3 V
25	RsvBus10	Reserved	A06	IRQ6*	A13	Reserved	RsvBus11
26	GND	GND	A05	IRQ5*	A12	Reserved	+3.3 V
27	RsvBus12	Reserved	A04	IRQ4*	A11	Reserved	LI\I*
28	GND	GND	A03	IRQ3*	A10	Reserved	+3.3 V
29	SBB	Reserved	A02	IRQ2*	A09	Reserved	LI\O*
30	GND	GND	A01	IRQ1*	A08	Reserved	+3.3 V
31	SBA	Reserved	-12 V	+5 V STDBY	+12 V	Reserved	GND
32	GND	GND	+5 V	+5 V	+5 V	Reserved	VPC

* low-active

VME, VME64 and VME64x
Pin Assignments
Accessories

Pin Assignments J2

Pin	ROW Z		ROW A VME	ROW B VME	ROW C VME	ROW D	
	VME64x	VME64				VME64	VME64x
1	User Defined	Reserved	User Defined	+5 V	User Defined	Reserved	User Defined
2	GND	GND	User Defined	GND	User Defined	Reserved	User Defined
3	User Defined	Reserved	User Defined	RETRY*	User Defined	Reserved	User Defined
4	GND	GND	User Defined	A24	User Defined	Reserved	User Defined
5	User Defined	Reserved	User Defined	A25	User Defined	Reserved	User Defined
6	GND	GND	User Defined	A26	User Defined	Reserved	User Defined
7	User Defined	Reserved	User Defined	A27	User Defined	Reserved	User Defined
8	GND	GND	User Defined	A28	User Defined	Reserved	User Defined
9	User Defined	Reserved	User Defined	A29	User Defined	Reserved	User Defined
10	GND	GND	User Defined	A30	User Defined	Reserved	User Defined
11	User Defined	Reserved	User Defined	A31	User Defined	Reserved	User Defined
12	GND	GND	User Defined	GND	User Defined	Reserved	User Defined
13	User Defined	Reserved	User Defined	+5 V	User Defined	Reserved	User Defined
14	GND	GND	User Defined	D16	User Defined	Reserved	User Defined
15	User Defined	Reserved	User Defined	D17	User Defined	Reserved	User Defined
16	GND	GND	User Defined	D18	User Defined	Reserved	User Defined
17	User Defined	Reserved	User Defined	D19	User Defined	Reserved	User Defined
18	GND	GND	User Defined	D20	User Defined	Reserved	User Defined
19	User Defined	Reserved	User Defined	D21	User Defined	Reserved	User Defined
20	GND	GND	User Defined	D22	User Defined	Reserved	User Defined
21	User Defined	Reserved	User Defined	D23	User Defined	Reserved	User Defined
22	GND	GND	User Defined	GND	User Defined	Reserved	User Defined
23	User Defined	Reserved	User Defined	D24	User Defined	Reserved	User Defined
24	GND	GND	User Defined	D25	User Defined	Reserved	User Defined
25	User Defined	Reserved	User Defined	D26	User Defined	Reserved	User Defined
26	GND	GND	User Defined	D27	User Defined	Reserved	User Defined
27	User Defined	Reserved	User Defined	D28	User Defined	Reserved	User Defined
28	GND	GND	User Defined	D29	User Defined	Reserved	User Defined
29	User Defined	Reserved	User Defined	D30	User Defined	Reserved	User Defined
30	GND	GND	User Defined	D31	User Defined	Reserved	User Defined
31	User Defined	Reserved	User Defined	GND	User Defined	Reserved	GND
32	GND	GND	User Defined	+5 V	User Defined	Reserved	VPC

* low-active

Accessories - Order numbers

F006.00550	cables for 7-pin utility connector 2.54 mm, l = 50 cm
F006.00004	cables for 10-pin utility connector 2.54 mm, l = 50 cm
F006.00450	cables for 14-pin utility connector 2.54 mm, l = 50 cm

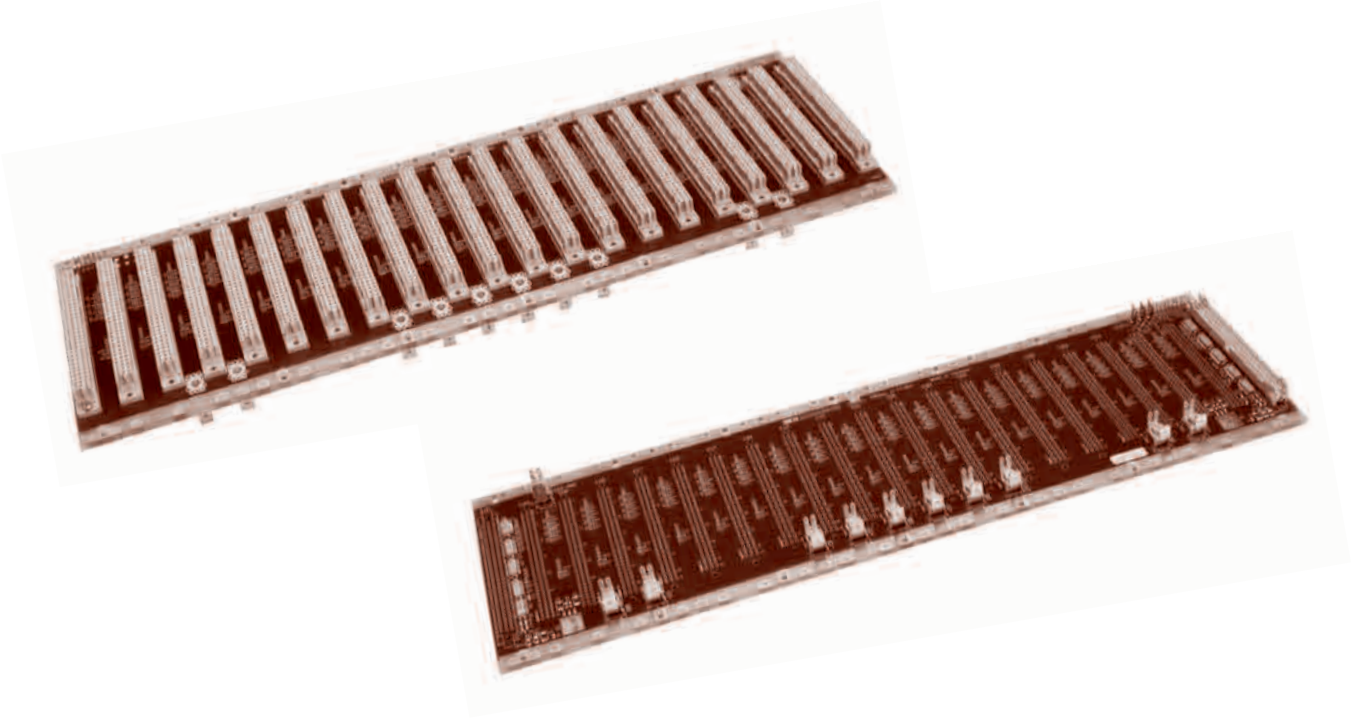
VME, VME64 and VME64x
Technical data

	VME J1	VME J1 / J2
Base material	Fiberglass epoxide acc. to DIN 40802 (type FR4)	
Layer structure	Optimized for best HF behavior. Outer layers designed as shielding areas.	
Ohmic resistance of signal lines	< 1.5 Ω	< 1.5 Ω
PCB thickness	3.2 mm	3.2 mm
Surge impedance Z of signal lines	60 Ω	55 Ω
Basic power consumption, both ends terminated	Active: Passive:	< 0.1 A < 1.0 A
		Active: < 0.2 A Passive: < 1.3 A
Power supply connection		
• Terminal bar with screw-type terminal M6	---	---
• Screw-type M4 and Faston 6.3 x 0.8 mm	X	---
• < 5 slots:	Faston 6.3 x 0.8 mm	---
• Permissible current loading of terminal bar	---	200 A
• Permissible current loading of a combined double spade/screw-type connection	25 A	25 A
• Permissible current loading of Faston connector	10 A	10 A
• Permissible current loading of assembly per slot	at +5 V 4.5 A at +12 V 1.5 A at –12 V 1.5 A at +5 VSTDBY 1.5 A	at +5 V 9.0 A at +12 V 1.5 A at –12 V 1.5 A at +5 VSTDBY 1.5 A
Termination ON/IN board	passive or active	passive or active
Installation height	3 HE/3 U	6 HE/6 U
Slot spacing	4 HP (different slot spacing upon request)	
Connectors	Press-fit quality class 2	
	96 pins DIN 41612	96 pins DIN 41612
Operating temperature range		
• Active termination	0 °C ... +70 °C	0 °C ... +70 °C
• Passive termination	–40 °C ... +80 °C	–40 °C ... +80 °C
Relative humidity	90 %, non-condensing	90 %, non-condensing

VME, VME64 and VME64x
Technical data

	VME64	VME64x
Base material	Fiberglass epoxide acc. to DIN 40802 (type FR4)	
Layer structure	Optimized for best HF behavior. Outer layers designed as shielding areas.	
Ohmic resistance of signal lines	< 1.5 Ω	< 1.5 Ω
PCB thickness	3.2 – 4.0 mm	4.3 mm
Surge impedance Z of signal lines	60 Ω	50 Ω
Basic power consumption, both ends terminated	Active: < 0.1 A Passive: < 1.4 A	Active: < 0.1 A Passive: < 1.6 A
Power supply connection		
• Terminal bar with screw-type terminal M6	X	X
• Screw-type M4 and Faston 6.3 x 0.8 mm	X	X
• < 5 slots:	Faston 6.3 x 0.8 mm	Faston 6.3 x 0.8 mm
• Permissible current loading of terminal bar	200 A	200 A
• Permissible current loading of a combined double spade/screw-type connection	25 A	25 A
• Permissible current loading of Faston connector	10 A	10 A
• Permissible current loading of assembly per slot	at +5 V 9.0 A at +12 V 1.5 A at –12 V 1.5 A at +5 V STDBY 1.5 A	at +3.3 V 12.5 A at +5 V 9.0 A at +12 V 1.5 A at –12 V 1.5 A at +5 V STDBY 1.5 A at +48 V (38-75 V) 3.0 A
Termination ON/IN board	passive or active	passive or active
Installation height	6 HE/6 U	3 HE/6 HE/6,5 HE 3 U/6 U/6.5 U
Slot spacing	4 HP (different slot spacing upon request)	
Connectors	Press-fit quality class 2	
	160 pins compatible with C96 ---	160 pins compatible with C96 optionally J0, spacing 2 mm 95 / 133 pins
Operating temperature range		
• Active termination	0 °C ... +70 °C	0 °C ... +70 °C
• Passive termination	–40 °C ... +80 °C	–40 °C ... +80 °C
Relative humidity	90 %, non-condensing	90 %, non-condensing

VMEbus J1
3 U
Series 129/130



Active or passive termination is possible with this VMEbus series.

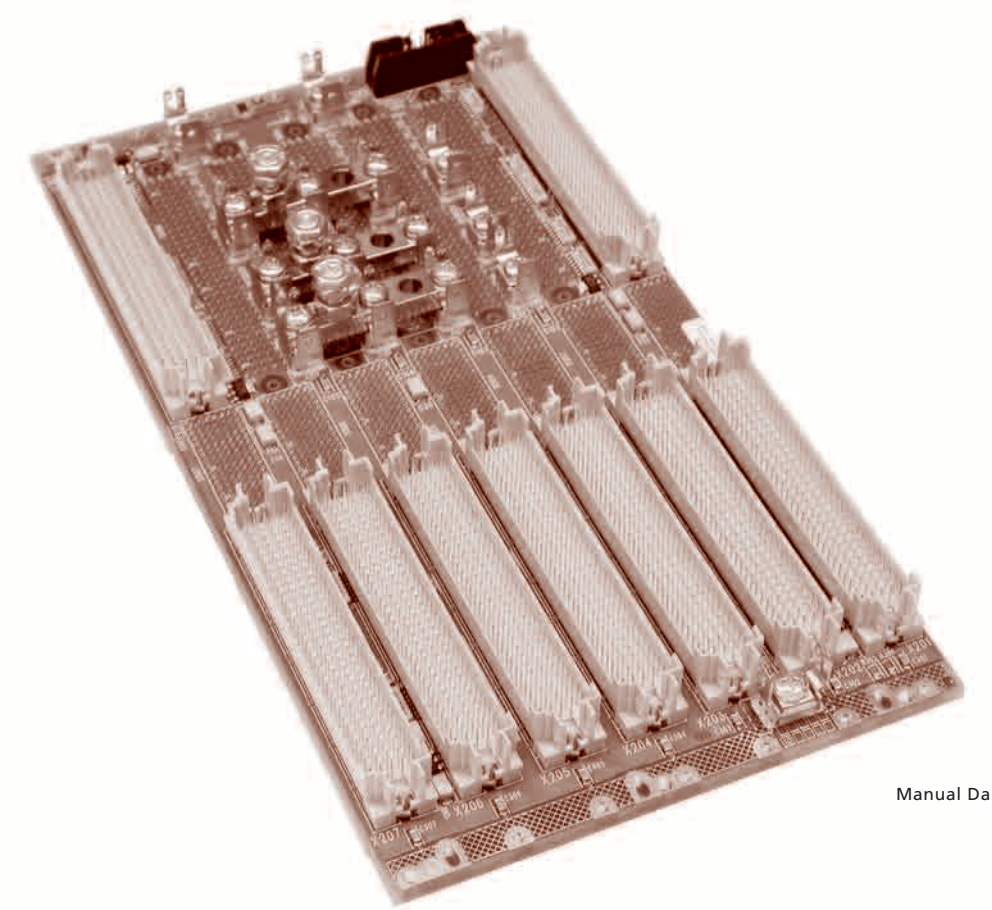
Electrically, the corresponding wiring is located at the end of the bus lines. Mechanically, it is situated between the outermost slots in a space-saving manner.

Order numbers

B1294 _ _ A7B	VME J1 3 U Manual daisy chain active termination
B1294 _ _ P7B	VME J1 3 U Manual daisy chain passive termination
B1294 _ _ A7D	VME J1 3 U Automatic daisy chain (with switching connectors) active termination
B1294 _ _ P7D	VME J1 3 U Automatic daisy chain (with switching connectors) passive termination
B1304 _ _ A7D	VME J1 3 U electronic Automatic daisy chain (with OR gate) active termination
B1304 _ _ P7D	VME J1 3 U electronic Automatic daisy chain (with OR gate) passive termination

_ _: No. of slots
(1 Slot = 4 HP = 20.32 mm)

VME64x
6 U
Series 166/167



Manual Daisy Chain

The VME64x is an extension of the VME family according to ANSI/VITA 1.1-1997 and permits 64-bit data traffic. This system is downward compatible, so that assemblies with 96-pin connectors to DIN 41612 can be inserted in the 160-pin socket connectors on the backplane.

Manual Daisy Chaining

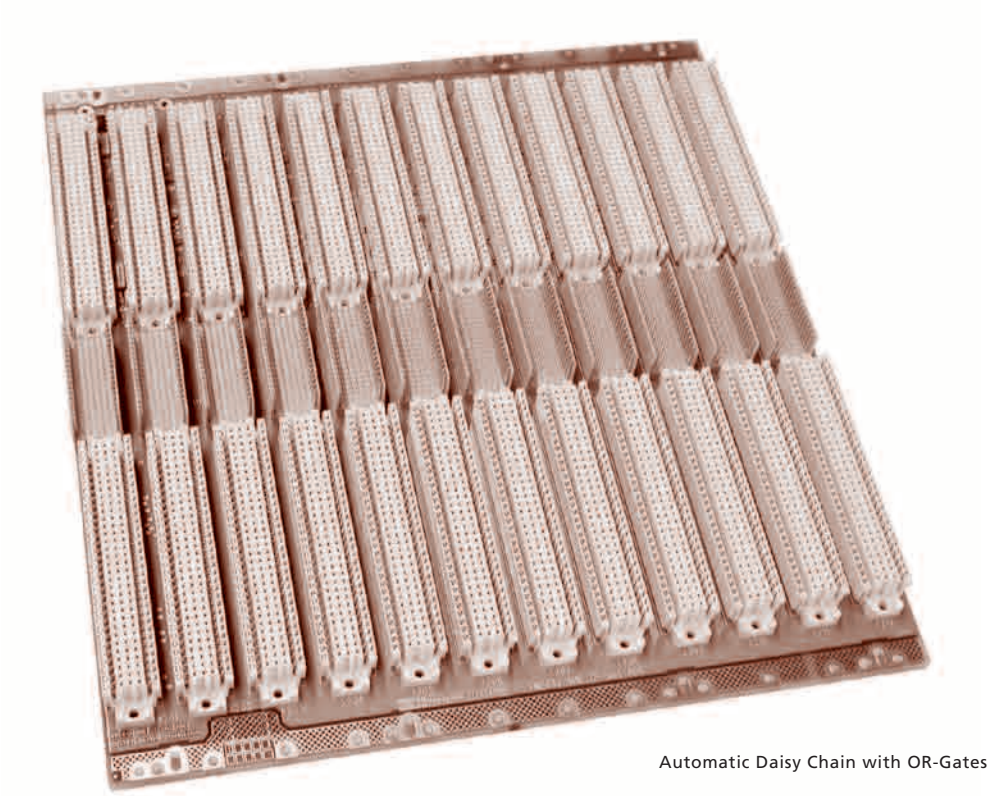
In the case of unused slots, the daisy chain signals can be bridged by means of jumpers or wire-wrap connections from the front or rear of the backplane.

Power is supplied via screw connections and terminal bars.

Automatic Daisy Chaining

Automatic daisy chain wiring with OR gates makes manual setting of jumpers unnecessary.

VME64x
6 U
Series 166/167



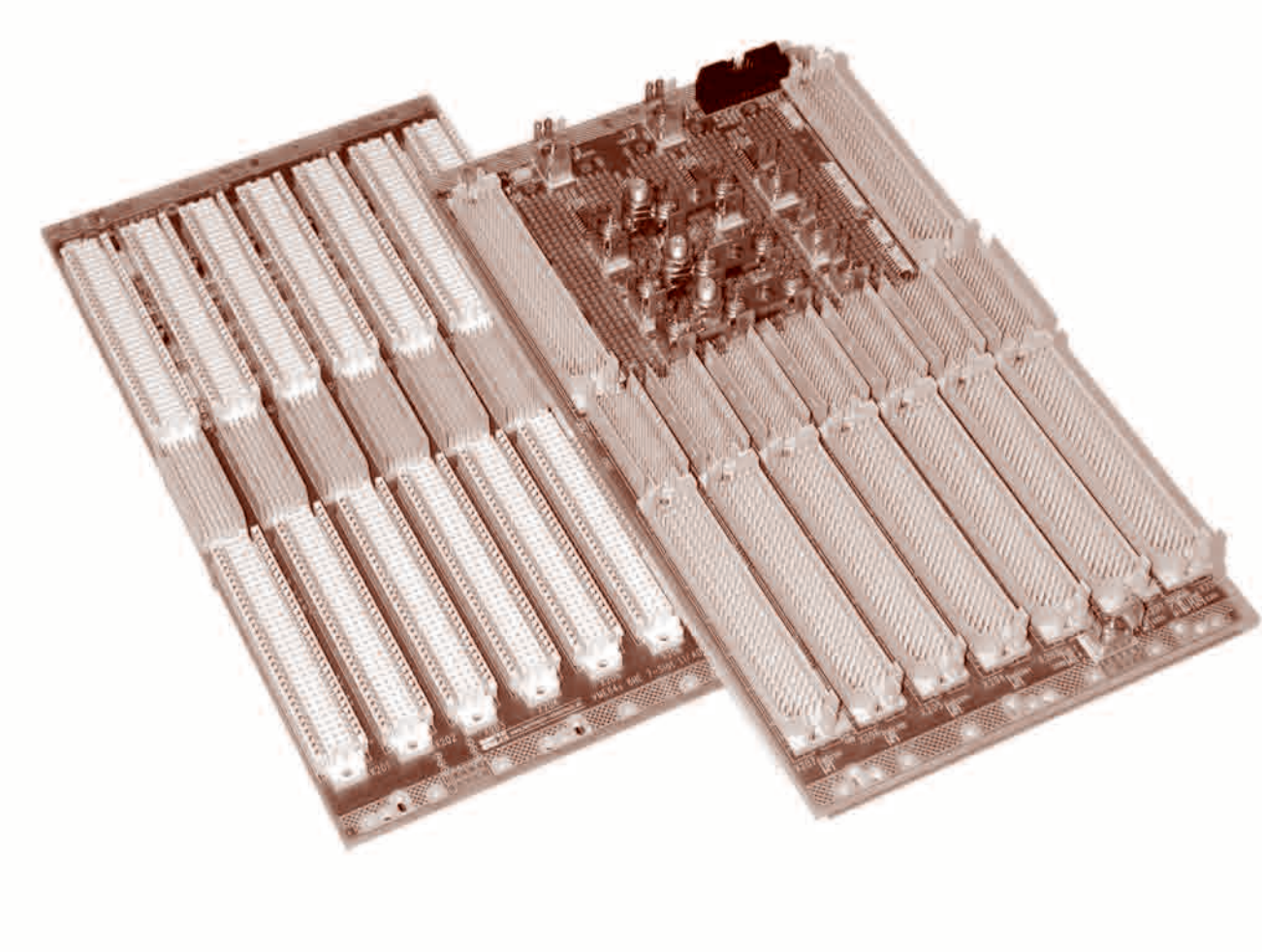
Automatic Daisy Chain with OR-Gates

Order numbers

B1664 _ _ A7B	VME64x 6 U J1/J2/J0 Manual daisy chain active termination
B1664 _ _ A8B	VME64x 6 U J1/J2 Manual daisy chain passive termination
B1664 _ _ A7D	VME64x 6 U J1/J2/J0 electronic Automatic daisy chain (with OR gate) active termination
B1664 _ _ A8D	VME64x 6 U J1/J2 electronic Automatic daisy chain (with OR gate) active termination
B1664 _ _ P7D	VME64x 6 U J1/J2/J0 electronic Automatic daisy chain (with OR gate) passive termination
B1664 _ _ P8D	VME64x 6 U J1/J2 electronic Automatic daisy chain (with OR gate) passive termination

_ _: No. of slots
(1 Slot = 4 HP = 20.32 mm)

VME64x
6 U
Series 166/167



Live Insertion and Automatic Daisy Chain

Live Insertion does not require additional modules; these have already been integrated in the backplane.

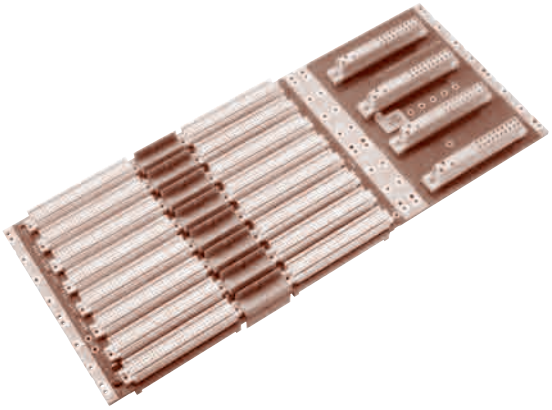
Automatic daisy chain wiring with OR gates makes manual setting of jumpers unnecessary.

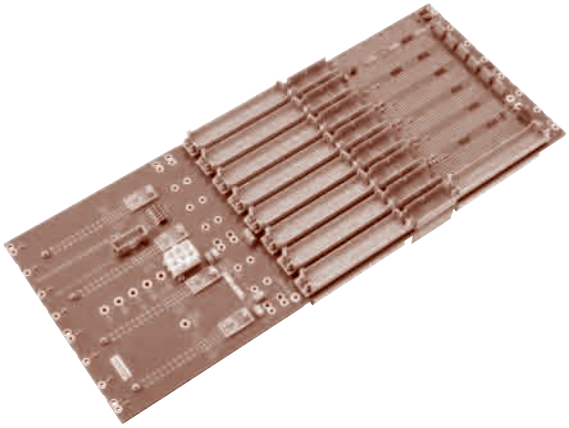
Order numbers

B1674 _ _ A7D	VME64x 6 U J1/J2/J0 electronic Automatic daisy chain (with OR gate) + Live Insertion active termination
B1674 _ _ A8D	VME64x 6 U J1/J2 electronic Automatic daisy chain (with OR gate) + Live Insertion active termination

_ _: No. of slots
(1 Slot = 4 HP = 20.32 mm)

VME64x
Backplane 6+3U
horizontal assembly





These backplanes are optimised for the assembly of horizontal systems with backplanes installed diagonally.

Electrical power supply by means of the P47 power plug-in connector.

To make the system assembly as easy as possible to configure, power monitoring with SysReset generation has been implemented. The FAL signal for the power supply units is provided to the VME bus as ACFAIL.

Temperature sensors and connection terminals for fans are also available.

A DIP switch facilitates selecting between two different characteristic temperature curves for each fan:

ON: reduced characteristic temperature curve
OFF: Standard characteristic temperature curve

For system assemblies with a fan slot, fan signals are also provided by a 14 pole plug.

Plug-in connecters for external connection of the JTAG and IPMB busses are also included as standard.

VME64x
Backplane 6+3U
horizontal assembly

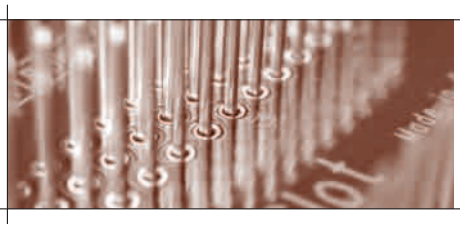
Pin assignment for the additional plugs

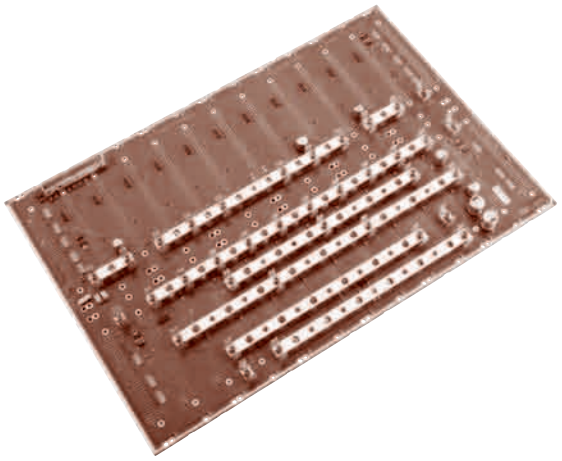
Pin	Fan connection terminal	Fan connection terminal X75 at 2.H0003020	Adapter for the fan slot	DIP switch for selection of the characteristic temperature curve
1	+12 V	+12 V	GND	Fan 1
2	GND	Fan_Load	+12 V	Fan 2
3	Fan_Load	GND	GND	Fan 3
4	Temperature sensor	Temperature sensor 1	+12 V	Fan 4
5		Temperature sensor 2	GND	Fan 5
6		Temperature sensor 3	+12 V	Fan 6
7			GND	
8			Fan_Load	
9			Temperature sensor 4	
10			Temperature sensor 1	
11			Temperature sensor 5	
12			Temperature sensor 2	
13			Temperature sensor 6	
14			Temperature sensor 3	

Order numbers

2.H0003020	VME64x J1/J2/J0 active 2 slots 9 U V(I/O) = 5 V 1*P47 for 1U system plattforms
2.H0006010	VME64x J1/J2/J0 active 4 slots 9 U V(I/O) = 5 V 2*P47 for 2U system plattforms
2.H0012010	VME64x J1/J2/J0 active 8 slots 9 U V(I/O) = 5 V 4*P47 for 4U system plattforms

VXI
6 U
General and technical information





The VMEbus, based on the IEEE 1014 and IEC 821 standards, has become an established industrial standard worldwide. The VXIbus (VMEbus Extensions for Instrumentation) extends the VME family based on System Specification VXI-1 Revision 3.0 from November 24, 2003.
All Hartmann VMEbus boards are based on the HIGH-SPEED DESIGN concept. Low reflection is achieved by means of uniform signal line surge impedance. Shielding of each individual signal line assures minimal coupling and therefore guarantees trouble-free operation.

Termination
In order to prevent interference on signal lines which might result from reflection at open line ends, these lines must be terminated. A distinction is made between passive and active termination. The advantage of active termination is reduced closed-circuit current consumption. Passive termination features better frequency response.

Automatic daisy chaining
For this VXI-Backplane daisy chaining is implemented using a integrated OR logic. This logic closes the daisy chain when the daughter board is removed.

Chassis GND connection
There is a solid electrically conductive chassis GND surface in the backplane-to-card rack mounting area.

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This guarantees EMC-tight mounting of the bus board on the card rack.

HF coupling of card rack and system ground is implemented for VXI by capacitors (10 nF, 200 V in each slot). Static charges are discharged with a resistor (≥ 1 MΩ).

Chassis-GND is connected with the Backplane with a contact area. Additional its possible to make a connection over a M4-terminal.

In case of using an extended terminal bar for GND its possible to connect the chassis directly with Digital-GND.Every Slot is shielded. There are 2 variants available: One is connecting the shield with Chassis-GND and the other with Digital-GND.

Power connections

The main operating voltages and GND are supplied via terminal bars with M6 screw connections.

The auxiliary operating voltages are supplied via M4 screw terminals with dual Fastons. Optimal daughter board supply and trouble-free operation are ensured by the arrangement of the feed modules on the backplane.

Utility connector

The special signals to the power supply unit are brought out to a separate connector on the backplane. Beside the lines for voltage monitoring 8 external connectors for temperature sensors are feed-through to the 40-pin connector.

All lines for voltage monitoring are connected with line filters. A double-row 40-pin connector with a contact spacing of 2.54 mm is used.

Power Management

There is an additional connector for IPMB on the backplane. IPMB_PWR is alternative accessible with an optional 3-pin feed-through contacts or with assembled zero-Ohm-resistors.

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Pin Assignments

Pin	1	2	3	4	5
IPMB (X66)	IPMB_SCL	GND	IPMB_SDA	IPMB_PWR	NC
IPMB_PWR (X68)	+5 V	IPMB_PWR	+5 VSTBY		

Pin	J1			Utility connector
	ROW A VME	ROW B VME	ROW C VME	
1	D00	BBSY*	D08	unused
2	D01	BCLR*	D09	unused
3	D02	ACFAIL*	D10	-12 V Sense
4	D03	BG0IN*	D11	-12 V Return
5	D04	BG0OUT*	D12	+12 V Sense
6	D05	BG1IN*	D13	+12 V Return
7	D06	BG1OUT*	D14	-24 V Sense
8	D07	BG2IN*	D15	-24 V Return
9	GND	BG2OUT*	GND	+24 V Sense
10	SYSCLK	BG3IN*	SYSFAIL*	+24 V Return
11	GND	BG3OUT*	BERR*	-2 V Sense
12	DS1*	BR0*	SYSRESET*	-2 V Return
13	DS0*	BR1*	LWORD*	-5.2 V Sense
14	WRITE*	BR2*	AM5	-5.2 V Return
15	GND	BR3*	A23	NC
16	DTACK*	AM0	A22	NC
17	GND	AM1	A21	NC
18	AS*	AM2	A20	NC
19	GND	AM3	A19	+5 V Sense
20	IACK*	GND	A18	+5 V Return
21	IACKIN*	IPMB_SCL	A17	SYSFAIL*
22	IACKOUT*	IPMB_SDA	A16	GND
23	AM4	GND	A15	ACFAIL*
24	A07	IRQ7*	A14	GND
25	A06	IRQ6*	A13	SYSRESET*
26	A05	IRQ5*	A12	GND
27	A04	IRQ4*	A11	NC
28	A03	IRQ3*	A10	NC
29	A02	IRQ2*	A09	Temp. 8
30	A01	IRQ1*	A08	Temp. 7
31	-12 V	+5 V STDBY	+12 V	Temp. 6
32	+5 V	+5 V	+5 V	Temp. 5
33				Temp. 4
34				Temp. 3
35				Temp. 2
36				Temp. 1
37				Temp. Return
38				NC
39				NC
40				NC

NC = not connected
* low-active

Pin Assignments J2

Pin	Slot 0			Slot 1 - 12		
	ROW A VXI	ROW B VME	ROW C VXI	ROW A VXI	ROW B VME	ROW C VXI
1	ECLTRG0	+5 V	CLK10+	ECLTRG0	+5 V	CLK10+
2	-2 V	GND	CLK10-	-2 V	GND	CLK10-
3	ECLTRG1	RETRY*	GND	ECLTRG1	RETRY*	GND
4	GND	A24	-5.2 V	GND	A24	-5.2 V
5	MODID12	A25	LBUSC00	LBUSA00	A25	LBUSC00
6	MODID11	A26	LBUSC01	LBUSA01	A26	LBUSC01
7	-5.2 V	A27	GND	-5.2 V	A27	GND
8	MODID10	A28	LBUSC02	LBUSA02	A28	LBUSC02
9	MODID09	A29	LBUSC03	LBUSA03	A29	LBUSC03
10	GND	A30	GND	GND	A30	GND
11	MODID08	A31	LBUSC04	LBUSA04	A31	LBUSC04
12	MODID07	GND	LBUSC05	LBUSA05	GND	LBUSC05
13	-5.2 V	+5 V	-2 V	-5.2 V	+5 V	-2 V
14	MODID06	D16	LBUSC06	LBUSA06	D16	LBUSC06
15	MODID05	D17	LBUSC07	LBUSA07	D17	LBUSC07
16	GND	D18	GND	GND	D18	GND
17	MODID04	D19	LBUSC08	LBUSA08	D19	LBUSC08
18	MODID03	D20	LBUSC09	LBUSA09	D20	LBUSC09
19	-5.2 V	D21	-5.2 V	-5.2 V	D21	-5.2 V
20	MODID02	D22	LBUSC10	LBUSA10	D22	LBUSC10
21	MODID01	D23	LBUSC11	LBUSA11	D23	LBUSC11
22	GND	GND	GND	GND	GND	GND
23	TTLTRG0*	D24	TTLTRG1*	TTLTRG0*	D24	TTLTRG1*
24	TTLTRG2*	D25	TTLTRG3*	TTLTRG2*	D25	TTLTRG3*
25	+5 V	D26	GND	+5 V	D26	GND
26	TTLTRG4*	D27	TTLTRG5*	TTLTRG4*	D27	TTLTRG5*
27	TTLTRG6*	D28	TTLTRG7*	TTLTRG6*	D28	TTLTRG7*
28	GND	D29	GND	GND	D29	GND
29	RSV2	D30	RSV3	RSV2	D30	RSV3
30	MODID00	D31	GND	MODID	D31	GND
31	GND	GND	+24 V	GND	GND	+24 V
32	SUMBUS	+5 V	-24 V	SUMBUS	+5 V	-24 V

* low-active

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Technical data

Base material	Fiberglass epoxide acc. to DIN 40802 (type FR4)
Layer structure	Optimized for best HF behavior. Outer layers designed as shielding areas.
Ohmic resistance of signal lines	< 1.0 Ω
PCB thickness	2.8 mm
Surge impedance Z of signal lines	60 Ω
Basic power consumption, both ends terminated	Active: < 0.1 A Passive 5 V: < 1.0 A
• Power supply connection: Terminal bar with screw-type terminal M6	X
• Permissible current loading of a combined double spade/screw-type connection	30 A
• Permissible current loading of assembly per slot	at +5 V 12.5 A at +12 V 3.7 A at –12 V 3.7 A at +24 V 2.8 A at –24 V 2.8 A at +5 VSTDBY 1.5 A at –5.2 V 9.5 A at +2 V 6.8 A
Termination	passive 5 V or active
Installation height	6 HE/6 U
Slot spacing	6 TE/6 HP
Connectors	Press-fit quality class 2 96 pins DIN 41612
Operating temperature range	0 °C ... +70 °C
Relative humidity	95 %, non-condensing

Order numbers

B173613A7D	VXI J1/J2 13 slots ACD/active shielding Chassis-GND
B173613P7D	VXI J1/J2 13 slots ACD/passive shielding Chassis-GND
B173613A8D	VXI J1/J2 13 slots ACD/active shielding Digital-GND
B173613P8D	VXI J1/J2 13 slots ACD/passive shielding Digital-GND

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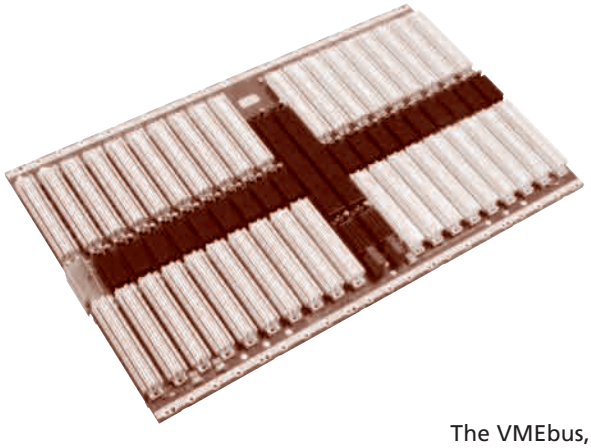

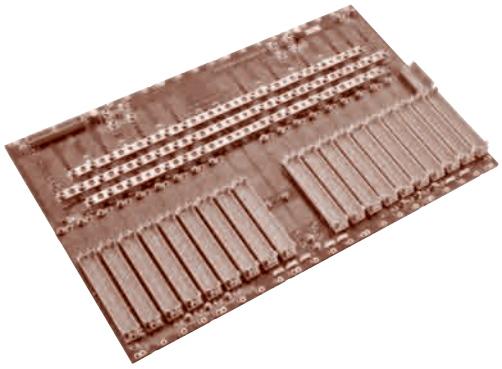

The VMEbus, based on the IEEE 1014 and IEC 821 standards, has become an established industrial standard worldwide.
The VXS (VMEbus Switched Serial Standard) represents an extension of the VME family according to VITA 41.0. This system is downward-compatible, so that assemblies with 96-pin connectors to DIN 41612 can still be used.
All Hartmann VMEbus boards are based on the HIGH-SPEED DESIGN concept. Low reflection is achieved by means of uniform signal line surge impedance. Shielding of each individual signal line assures minimal coupling and therefore guarantees trouble-free operation even when expanded to the 64-bit mode with the 2e protocol (160Mbyte/s).
The transmission capacity in the VXS range (J0) is 2500 Mbits/s for each pair of cards.

Termination

In order to prevent interference on signal lines which might result from reflection at open line ends, these lines must be terminated.
A distinction is made between passive and active termination. The advantage of active termination is reduced closed-circuit current consumption. Passive termination features better frequency response.

Daisy chaining wiring

For this VXS-Backplane automatic daisy-chaining with a patented bidirectional procedure (Wiener patente no. 102004023737.9 (Germany) und EP1745386 (Europe)) is used.

Chassis GND connection

There is a solid electrically conductive chassis GND surface in the backplane-to-card rack mounting area. This guarantees EMC-tight mounting of the bus board on the card rack.

HF coupling of card rack and system ground is implemented by capacitors (10nF, 200 V in each slot).

Static charges are discharged with a resistor (≥ 1 MΩ).

An additional Chassis-GND connection is provided with a M3 terminal screw.

Power connections

The main operating voltages and GND are supplied via terminal bars and M4 screws for the cables. On request additional M6 screw will be added.
V1/V2 is available via M4 screw terminals. They can be linked together with terminal bars.

The auxiliary operating voltages are supplied via M3 screw terminals. The arrangement of terminal bars ensures an optimal power supply of the modules.

Utility connector

The special signals to the power supply unit are brought out to a separate connector on the backplane. Beside the lines for Voltage Monitoring 8 external connectors for temperature sensors are feed-through to the 40-pin connector.

All lines for Voltage Monitoring are connected with Line Filters. A double-row 40-pin connector with a contact spacing of 2.54 mm is used.

Power Management

Further connectors are available for serial communication with 4 power supplies (PS1-PS4) and a DSP.

AUX_PWR is set to 5 V or 5 V STDBY with a 3-pin feed-through connector.

There are 2 connectors for system management IPMB and SMB.

IPMB_PWR and SMB_PWR is settable to 5 V or 5 V STDBY with 3-pin feed-through connectors.

Live-Insertion

Live-Insertion signals (LI-IN; LI-OUT) are available via 2-pin feed-through connectors.

Geographical Addressing J1 VME64x

Slot Number	GAP* Pin J1-D9	GA4* Pin J1-D17	GA3* Pin J1-D15	GA2* Pin J1-D13	GA1* Pin J1-D11	GA0* Pin J1-D10
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
10	GND	Open	GND	Open	GND	Open
11	Open	Open	GND	Open	GND	GND
12	GND	Open	GND	GND	Open	Open
13	Open	Open	GND	GND	Open	GND
14	Open	Open	GND	GND	GND	Open
15	GND	Open	GND	GND	GND	GND
16	Open	GND	Open	Open	Open	Open
17	GND	GND	Open	Open	Open	GND
18	GND	GND	Open	Open	GND	Open
19	Open	GND	Open	Open	GND	GND
20	GND	GND	Open	GND	Open	Open
21	Open	GND	Open	GND	Open	GND

Pin Assignments

Pin	DSP (X1105)	PWR (X1206)	PS1 (X1101)	PS2 (X1102)	PS3 (X1103)	PS4 (X1104)	IPMB (X66)
1	DSP_SCL	+5 V	PS1_SCL	PS2_SCL	PS3_SCL	PS4_SCL	IPMB_SCL
2	GND	AUX_PWR	GND	GND	GND	GND	GND
3	DSP_SDA	+5 V STDBY	PS1_SDA	PS2_SDA	PS3_SDA	PS4_SDA	IPMB_SDA
4	AUX_PWR		AUX_PWR	AUX_PWR	AUX_PWR	AUX_PWR	IPMB_PWR
5	DSP_ALERT		PS1_ALERT	PS2_ALERT	PS3_ALERT	PS4_ALERT	SMB_ALERT

Pin	IPMB_PWR (X68)	SMB (X65)	SMB_PWR (X67)	LI-IN (XI01-21)	LI-OUT (X01-10, X13-20)	VXS_PWR (X11_P, X12_P)
1	+5 V	SMB_SCL	+5 V	LI\I*	LI\O*	VPC
2	IPMB_PWR	GND	SMB_PWR	GND	GND	VPC
3	+5 V STDBY	SMB_SDA	+5 V STDBY			VPC
4		SMB_PWR				VPC
5		SMB_ALERT				GND
6						GND

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Pin Assignment Utility connector X5

Pin	1	2	3	4	5	6	7	8	9	10
	+3.3 V Sense	-3.3 V Return	-12 V Sense	-12 V Return	+12 V Sense	+12 V Return	-48 V Sense 2	+48 V Sense 2	+48 V Sense 1	-48 V Sense 1

Pin	11	12	13	14	15	16	17	18	19	20
	NC	NC	NC	NC	NC	NC	NC	NC	+5 V Sense	+5 V Return

Pin	21	22	23	24	25	26	27	28	29	30
	SYSFAIL*	GND	ACFAIL*	GND	SYSRESET*	GND	NC	NC	Temp. 8	Temp. 7

Pin	31	32	33	34	35	36	37	38	39	40
	Temp. 6	Temp. 5	Temp. 4	Temp. 3	Temp. 2	Temp. 1	Temp. Return	NC	NC	NC

NC = not connected

Pin Assignments J1 VME64x

Pin	ROW Z	ROW A	ROW B	ROW C	ROW D - Slot 1	ROW D
1	MPR	D00	BBSY*	D08	VPC	VPC
2	GND	D01	BCLR*	D09	GND	GND
3	MCLK	D02	ACFAIL*	D10	+V1	+V1
4	GND	D03	BG0IN*	D11	+V2	+V2
5	MSD	D04	BG0OUT*	D12	RsvU-1	RsvU-1
6	GND	D05	BG1IN*	D13	-V1	-V1
7	MMD	D06	BG1OUT*	D14	-V2	-V2
8	GND	D07	BG2IN*	D15	RsvU-2	RsvU-2
9	MCTL	GND	BG2OUT*	GND	GAP*	GAP*
10	GND	SYSCLK	BG3IN*	SYSFAIL*	GA0*	GA0*
11	RESP*	GND	BG3OUT*	BERR*	GA1*	GA1*
12	GND	DS1*	BR0*	SYSRESET*	+3.3 V	+3.3 V
13	RsvBus1	DS0*	BR1*	LWORD*	GA2*	GA2*
14	GND	WRITE*	BR2*	AM5	+3.3 V	+3.3 V
15	RsvBus2	GND	BR3*	A23	GA3*	GA3*
16	GND	DTACK*	AM0	A22	+3.3 V	+3.3 V
17	RsvBus3	GND	AM1	A21	GA4*	GA4*
18	GND	AS*	AM2	A20	+3.3 V	+3.3 V
19	RsvBus4	GND	AM3	A19	SMB_SCL	RsvBus5
20	GND	IACK*	GND	A18	+3.3 V	+3.3 V
21	RsvBus6	IACKIN*	IPMB_SCL	A17	SMB_SDA	RsvBus7
22	GND	IACKOUT*	IPMB_SDA	A16	+3.3 V	+3.3 V
23	RsvBus8	AM4	GND	A15	SMB_ALERT*	RsvBus9
24	GND	A07	IRQ7*	A14	+3.3 V	+3.3 V
25	RsvBus10	A06	IRQ6*	A13	RsvBus11	RsvBus11
26	GND	A05	IRQ5*	A12	+3.3 V	+3.3 V
27	RsvBus12	A04	IRQ4*	A11	LI\I*	LI\I*
28	GND	A03	IRQ3*	A10	+3.3 V	+3.3 V
29	RsvBus13	A02	IRQ2*	A09	LI\O*	LI\O*
30	GND	A01	IRQ1*	A08	+3.3 V	+3.3 V
31	RsvBus14	-12 V	+5 V STDBY	+12 V	GND	GND
32	GND	+5 V	+5 V	+5 V	VPC	VPC

* low-active

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Pin Assignments J2 VME64x

Pin	ROW Z	ROW A	ROW B	ROW C	ROW D
1	User Defined	User Defined	+5 V	User Defined	User Defined
2	GND	User Defined	GND	User Defined	User Defined
3	User Defined	User Defined	RETRY*	User Defined	User Defined
4	GND	User Defined	A24	User Defined	User Defined
5	User Defined	User Defined	A25	User Defined	User Defined
6	GND	User Defined	A26	User Defined	User Defined
7	User Defined	User Defined	A27	User Defined	User Defined
8	GND	User Defined	A28	User Defined	User Defined
9	User Defined	User Defined	A29	User Defined	User Defined
10	GND	User Defined	A30	User Defined	User Defined
11	User Defined	User Defined	A31	User Defined	User Defined
12	GND	User Defined	GND	User Defined	User Defined
13	User Defined	User Defined	+5 V	User Defined	User Defined
14	GND	User Defined	D16	User Defined	User Defined
15	User Defined	User Defined	D17	User Defined	User Defined
16	GND	User Defined	D18	User Defined	User Defined
17	User Defined	User Defined	D19	User Defined	User Defined
18	GND	User Defined	D20	User Defined	User Defined
19	User Defined	User Defined	D21	User Defined	User Defined
20	GND	User Defined	D22	User Defined	User Defined
21	User Defined	User Defined	D23	User Defined	User Defined
22	GND	User Defined	GND	User Defined	User Defined
23	User Defined	User Defined	D24	User Defined	User Defined
24	GND	User Defined	D25	User Defined	User Defined
25	User Defined	User Defined	D26	User Defined	User Defined
26	GND	User Defined	D27	User Defined	User Defined
27	User Defined	User Defined	D28	User Defined	User Defined
28	GND	User Defined	D29	User Defined	User Defined
29	User Defined	User Defined	D30	User Defined	User Defined
30	GND	User Defined	D31	User Defined	User Defined
31	User Defined	User Defined	GND	User Defined	GND
32	GND	User Defined	+5 V	User Defined	VPC

Pin Assignments J0 VXS Payload

Pin	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F	ROW G	ROW H	ROW I
1	PA-RX0+	PA-RX0-	GND	GND	PA-TX0+	PA-TX0+	GND	GND	PA_SCL
2	GND	GND	PA-RX1+	PA-RX1-	GND	GND	PA-TX1+	PA-TX1+	GND
3	PA-RX2+	PA-RX2-	GND	GND	PA-TX2+	PA-TX2+	GND	GND	PA_SDA
4	GND	GND	PA-RX3+	PA-RX3-	GND	GND	PA-TX3+	PA-TX3+	GND
5	RFU	RFU	GND	GND	RFU	RFU	GND	GND	RFU
6	GND	GND	RFU	RFU	GND	GND	RFU	RFU	GND
7	RFU	RFU	GND	GND	RFU	RFU	GND	GND	RFU
8	GND	GND	RFU	RFU	GND	GND	RFU	RFU	GND
9	RFU	RFU	GND	GND	RFU	RFU	GND	GND	RFU
10	GND	GND	RFU	RFU	GND	GND	RFU	RFU	GND
11	RFU	RFU	GND	GND	RFU	RFU	GND	GND	PEN*
12	GND	GND	PB-RX0+	PB-RX0-	GND	GND	PB-TX0+	PB-TX0+	GND
13	PB-RX1+	PB-RX1-	GND	GND	PB-TX1+	PB-TX1+	GND	GND	PB_SCL
14	GND	GND	PB-RX2+	PB-RX2-	GND	GND	PB-TX2+	PB-TX2+	GND
15	PB-RX3+	PB-RX3-	GND	GND	PB-TX3+	PB-TX3+	GND	GND	PB_SCL

* low-active

VXS
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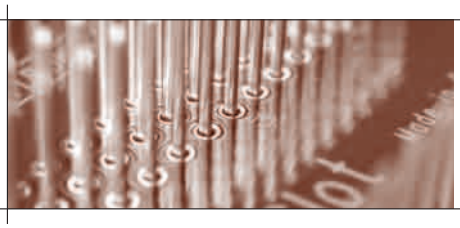
General and technical information



The pin assignments J0 VXS Payload is used for VXS 4X Infiniband protocol (ANSI/VITA 41.1) and VXS 4X Serial RapidIO protocol (ANSI/VITA 41.2).

Pin Assignments J2 VXS Switch Slot

Pin	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F	ROW G	ROW H	ROW I
1	PP12-RX0+	PP12-RX0-	GND	PP12-TX0+	PP12-TX0-	GND	SP4-TX0+	SP4-TX0-	GND
2	GND	PP12-RX1+	PP12-RX1-	GND	PP12-TX1+	PP12-TX1-	GND	SP4-TX1+	SP4-TX1-
3	PP12-RX2+	PP12-RX2-	GND	PP12-TX2+	PP12-TX2-	GND	SP4-TX2+	SP4-TX2-	GND
4	GND	PP12-RX3+	PP12-RX3-	GND	PP12-TX3+	PP12-TX3-	GND	SP4-TX3+	SP4-TX3-
5	PP14-RX0+	PP14-RX0-	GND	PP14-TX0+	PP14-TX0-	GND	SP4-RX0+	SP4-RX0-	GND
6	GND	PP14-RX1+	PP14-RX1-	GND	PP14-TX1+	PP14-TX1-	GND	SP4-RX1+	SP4-RX1-
7	PP14-RX2+	PP14-RX2-	GND	PP14-TX2+	PP14-TX2-	GND	SP4-RX2+	SP4-RX2-	GND
8	GND	PP14-RX3+	PP14-RX3-	GND	PP14-TX3+	PP14-TX3-	GND	SP4-RX3+	SP4-RX3-
9	PP16-RX0+	PP16-RX0-	GND	PP16-TX0+	PP16-TX0-	GND	RFU	RFU	GND
10	GND	PP16-RX1+	PP16-RX1-	GND	PP16-TX1+	PP16-TX1-	GND	RFU	RFU
11	PP16-RX2+	PP16-RX2-	GND	PP16-TX2+	PP16-TX2-	GND	RFU	RFU	GND
12	GND	PP16-RX3+	PP16-RX3-	GND	PP16-TX3+	PP16-TX3-	GND	RFU	RFU
13	PP18-RX0+	PP18-RX0-	GND	PP18-TX0+	PP18-TX0-	GND	RFU	RFU	GND
14	GND	PP18-RX1+	PP18-RX1-	GND	PP18-TX1+	PP18-TX1-	GND	RFU	RFU
15	PP18-RX2+	PP18-RX2-	GND	PP18-TX2+	PP18-TX2-	GND	RFU	RFU	GND
16	GND	PP18-RX3+	PP18-RX3-	GND	PP18-TX3+	PP18-TX3-	GND	RFU	RFU

Pin Assignments J3 VXS Switch Slot

Pin	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F	ROW G	ROW H	ROW I
1	PP2-RX0+	PP2-RX0-	GND	PP2-TX0+	PP2-TX0-	GND	SP2-TX0+	SP2-TX0-	GND
2	GND	PP2-RX1+	PP2-RX1-	GND	PP2-TX1+	PP2-TX1-	GND	SP2-TX1+	SP2-TX1-
3	PP2-RX2+	PP2-RX2-	GND	PP2-TX2+	PP2-TX2-	GND	SP2-TX2+	SP2-TX2-	GND
4	GND	PP2-RX3+	PP2-RX3-	GND	PP2-TX3+	PP2-TX3-	GND	SP2-TX3+	SP2-TX3-
5	PP4-RX0+	PP4-RX0-	GND	PP4-TX0+	PP4-TX0-	GND	SP2-RX0+	SP2-RX0-	GND
6	GND	PP4-RX1+	PP4-RX1-	GND	PP4-TX1+	PP4-TX1-	GND	SP2-RX1+	SP2-RX1-
7	PP4-RX2+	PP4-RX2-	GND	PP4-TX2+	PP4-TX2-	GND	SP2-RX2+	SP2-RX2-	GND
8	GND	PP4-RX3+	PP4-RX3-	GND	PP4-TX3+	PP4-TX3-	GND	SP2-RX3+	SP2-RX3-
9	PP8-RX0+	PP8-RX0-	GND	PP8-TX0+	PP8-TX0-	GND	PP6-TX0+	PP6-TX0-	GND
10	GND	PP8-RX1+	PP8-RX1-	GND	PP8-TX1+	PP8-TX1-	GND	PP6-TX1+	PP6-TX1-
11	PP8-RX2+	PP8-RX2-	GND	PP8-TX2+	PP8-TX2-	GND	PP6-TX2+	PP6-TX2-	GND
12	GND	PP8-RX3+	PP8-RX3-	GND	PP8-TX3+	PP8-TX3-	GND	PP6-TX3+	PP6-TX3-
13	PP10-RX0+	PP10-RX0-	GND	PP10-TX0+	PP10-TX0-	GND	PP6-RX0+	PP6-RX0-	GND
14	GND	PP10-RX1+	PP10-RX1-	GND	PP10-TX1+	PP10-TX1-	GND	PP6-RX1+	PP6-RX1-
15	PP10-RX2+	PP10-RX2-	GND	PP10-TX2+	PP10-TX2-	GND	PP6-RX2+	PP6-RX2-	GND
16	GND	PP10-RX3+	PP10-RX3-	GND	PP10-TX3+	PP10-TX3-	GND	PP6-RX3+	PP6-RX3-

Pin Assignments J4 VXS Switch Slot

Pin	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F	ROW G	ROW H	ROW I
1	PP9-RX0+	PP9-RX0-	GND	PP9-TX0+	PP9-TX0-	GND	PP5-TX0+	PP5-TX0-	GND
2	GND	PP9-RX1+	PP9-RX1-	GND	PP9-TX1+	PP9-TX1-	GND	PP5-TX1+	PP5-TX1-
3	PP9-RX2+	PP9-RX2-	GND	PP9-TX2+	PP9-TX2-	GND	PP5-TX2+	PP5-TX2-	GND
4	GND	PP9-RX3+	PP9-RX3-	GND	PP9-TX3+	PP9-TX3-	GND	PP5-TX3+	PP5-TX3-
5	PP7-RX0+	PP7-RX0-	GND	PP7-TX0+	PP7-TX0-	GND	PP5-RX0+	PP5-RX0-	GND
6	GND	PP7-RX1+	PP7-RX1-	GND	PP7-TX1+	PP7-TX1-	GND	PP5-RX1+	PP5-RX1-
7	PP7-RX2+	PP7-RX2-	GND	PP7-TX2+	PP7-TX2-	GND	PP5-RX2+	PP5-RX2-	GND
8	GND	PP7-RX3+	PP7-RX3-	GND	PP7-TX3+	PP7-TX3-	GND	PP5-RX3+	PP5-RX3-
9	PP3-RX0+	PP3-RX0-	GND	PP3-TX0+	PP3-TX0-	GND	SP1-TX0+	SP1-TX0-	GND
10	GND	PP3-RX1+	PP3-RX1-	GND	PP3-TX1+	PP3-TX1-	GND	SP1-TX1+	SP1-TX1-
11	PP3-RX2+	PP3-RX2-	GND	PP3-TX2+	PP3-TX2-	GND	SP1-TX2+	SP1-TX2-	GND
12	GND	PP3-RX3+	PP3-RX3-	GND	PP3-TX3+	PP3-TX3-	GND	SP1-TX3+	SP1-TX3-
13	PP1-RX0+	PP1-RX0-	GND	PP1-TX0+	PP1-TX0-	GND	SP1-RX0+	SP1-RX0-	GND
14	GND	PP1-RX1+	PP1-RX1-	GND	PP1-TX1+	PP1-TX1-	GND	SP1-RX1+	SP1-RX1-
15	PP1-RX2+	PP1-RX2-	GND	PP1-TX2+	PP1-TX2-	GND	SP1-RX2+	SP1-RX2-	GND
16	GND	PP1-RX3+	PP1-RX3-	GND	PP1-TX3+	PP1-TX3-	GND	SP1-RX3+	SP1-RX3-

Pin Assignments J5 VXS Switch Slot

Pin	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F	ROW G	ROW H	ROW I
1	PP17-RX0+	PP17-RX0-	GND	PP17-TX0+	PP17-TX0-	GND	RFU	RFU	GND
2	GND	PP17-RX1+	PP17-RX1-	GND	PP17-TX1+	PP17-TX1-	GND	RFU	RFU
3	PP17-RX2+	PP17-RX2-	GND	PP17-TX2+	PP17-TX2-	GND	RFU	RFU	GND
4	GND	PP17-RX3+	PP17-RX3-	GND	PP17-TX3+	PP17-TX3-	GND	RFU	RFU
5	PP15-RX0+	PP15-RX0-	GND	PP15-TX0+	PP15-TX0-	GND	RFU	RFU	GND
6	GND	PP15-RX1+	PP15-RX1-	GND	PP15-TX1+	PP15-TX1-	GND	RFU	RFU
7	PP15-RX2+	PP15-RX2-	GND	PP15-TX2+	PP15-TX2-	GND	RFU	RFU	GND
8	GND	PP15-RX3+	PP15-RX3-	GND	PP15-TX3+	PP15-TX3-	GND	RFU	RFU
9	PP13-RX0+	PP13-RX0-	GND	PP13-TX0+	PP13-TX0-	GND	SP3-TX0+	SP3-TX0-	GND
10	GND	PP13-RX1+	PP13-RX1-	GND	PP13-TX1+	PP13-TX1-	GND	SP3-TX1+	SP3-TX1-
11	PP13-RX2+	PP13-RX2-	GND	PP13-TX2+	PP13-TX2-	GND	SP3-TX2+	SP3-TX2-	GND
12	GND	PP13-RX3+	PP13-RX3-	GND	PP13-TX3+	PP13-TX3-	GND	SP3-TX3+	SP3-TX3-
13	PP11-RX0+	PP11-RX0-	GND	PP11-TX0+	PP11-TX0-	GND	SP3-RX0+	SP3-RX0-	GND
14	GND	PP11-RX1+	PP11-RX1-	GND	PP11-TX1+	PP11-TX1-	GND	SP3-RX1+	SP3-RX1-
15	PP11-RX2+	PP11-RX2-	GND	PP11-TX2+	PP11-TX2-	GND	SP3-RX2+	SP3-RX2-	GND
16	GND	PP11-RX3+	PP11-RX3-	GND	PP11-TX3+	PP11-TX3-	GND	SP3-RX3+	SP3-RX3-

Backplane Keying

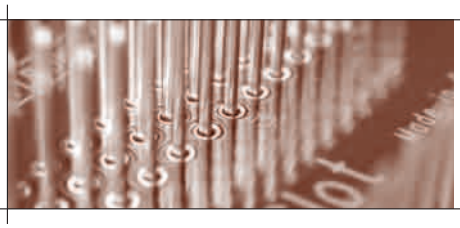
Playload slots (IEC Key K0) and
Switch slots (IEC Key K1):

KeyCode	Protocol	Color
1567	InfiniBand 4X	Brilliant Blue
3568	Serial RapidIO 4X	Pale Orange

Switch Slots (IEC Key K2):

KeyCode	Color	Protocol
2578	Reseda green	Switch board has no connector in User-IO area

VXS
6 U
Technical data



	VME64x J1	VXS J0, Switch Slot
Base material	Fiberglass epoxide acc. to DIN 40802 (type FR408 or NE4000-13)	
Layer structure	Optimized for best HF behavior. Outer layers designed as shielding areas.	
Ohmic resistance of signal lines	< 1.0 Ω	
PCB thickness	5.0 mm	
Surge impedance Z of signal lines	60 Ω	100 Ω
Basic power consumption, both ends terminated	Active: < 0.1 A Passive: < 1.4 A	
• Power supply connection: screw-type terminal M3 and M4	X	
• Permissible current loading of a screw-type connection M4	30 A	
• Permissible current loading of assembly per slot	at +3.3 V 12.5 A at +5 V 9.0 A at +12 V 1.5 A at –12 V 1.5 A at +48 V 3.0 A at –48 V 3.0 A at +5 VSTDBY 1.5 A	
Termination	passive 3.3 V, passive 5 V or active	
Installation height	6 HE/6 U	
Slot spacing	4 TE/4 HP	
Connectors	Press-fit quality class 2	
	160 pins IEC 61076-4-113	MultiGig RT2
Operating temperature range		
• Active termination	-40 °C ... +85 °C	
• Passive termination 3.3 V	-40 °C ... +85 °C	
• Passive termination 5 V	-40 °C ... +70 °C	
Relative humidity	95 %, non-condensing	

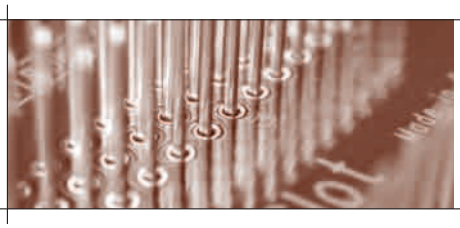
VXS
6 U
1 VME64x slot, 6 VXS slots and 1 switch slot

VXS-Backplanes with 1 VME64x slot, 6 VXS slots and 1 switch slot are available in following standard variants. This variant can be installed hoizontally.

Order numbers

B18106132I	VXS 6 Slot + 1*Switch + 1*VME64x InfiniBand active
B18106142I	VXS 6 Slot + 1*Switch + 1*VME64x InfiniBand active with Rear I/O on VXS J0
B18106132R	VXS 6 Slot + 1*Switch + 1*VME64x Serial RapidIO active
B18106142R	VXS 6 Slot + 1*Switch + 1*VME64x Serial RapidIO active with Rear I/O on VXS J0
B18106133I	VXS 6 Slot + 1*Switch + 1*VME64x InfiniBand passive 3.3 V
B18106143I	VXS 6 Slot + 1*Switch + 1*VME64x InfiniBand passive 3.3 V with Rear I/O on VXS J0
B18106123R	VXS 6 Slot + 1*Switch + 1*VME64x Serial RapidIO passive 3.3 V
B18106143R	VXS 6 Slot + 1*Switch + 1*VME64x Serial RapidIO passive 3.3 V with Rear I/O on VXS J0
B18106135I	VXS 6 Slot + 1*Switch + 1*VME64x InfiniBand passive 5 V
B18106145I	VXS 6 Slot + 1*Switch + 1*VME64x InfiniBand passive 5 V with Rear I/O on VXS J0
B18106135R	VXS 6 Slot + 1*Switch + 1*VME64x Serial RapidIO passive 5 V
B18106145R	VXS 6 Slot + 1*Switch + 1*VME64x Serial RapidIO passive 5 V with Rear I/O on VXS J0

VXS
6 U
1 VME64x slot, 9 VXS slots and 1 switch slot



VXS-Backplanes with 1 VME64x slot, 9 VXS slots and 1 switch slot are available in following standard variants:

Order numbers	
B18109132I	VXS 9 Slot + 1*Switch + 1*VME64x InfiniBand active
B18109142I	VXS 9 Slot + 1*Switch + 1*VME64x InfiniBand active with Rear I/O on VXS J0
B18109132R	VXS 9 Slot + 1*Switch + 1*VME64x Serial RapidIO active
B18109142R	VXS 9 Slot + 1*Switch + 1*VME64x Serial RapidIO active with Rear I/O on VXS J0
B18109133I	VXS 9 Slot + 1*Switch + 1*VME64x InfiniBand passive 3.3 V
B18109143I	VXS 9 Slot + 1*Switch + 1*VME64x InfiniBand passive 3.3 V with Rear I/O on VXS J0
B18109123R	VXS 9 Slot + 1*Switch + 1*VME64x Serial RapidIO passive 3.3 V
B18109143R	VXS 9 Slot + 1*Switch + 1*VME64x Serial RapidIO passive 3.3 V with Rear I/O on VXS J0
B18109135I	VXS 9 Slot + 1*Switch + 1*VME64x InfiniBand passive 5 V
B18109145I	VXS 9 Slot + 1*Switch + 1*VME64x InfiniBand passive 5 V with Rear I/O on VXS J0
B18109135R	VXS 9 Slot + 1*Switch + 1*VME64x Serial RapidIO passive 5 V
B18109145R	VXS 9 Slot + 1*Switch + 1*VME64x Serial RapidIO passive 5 V with Rear I/O on VXS J0

VXS
6 U
1 VME64x slot, 18 VXS slots and 2 switch slots

VXS-Backplanes with 1 VME64x slot, 18 VXS slots and 2 switch slots are available in following standard variants:

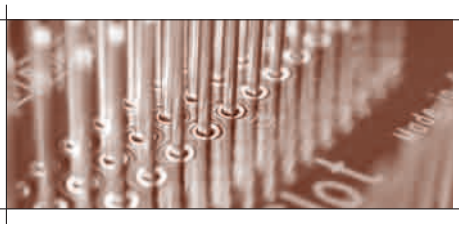
Order numbers

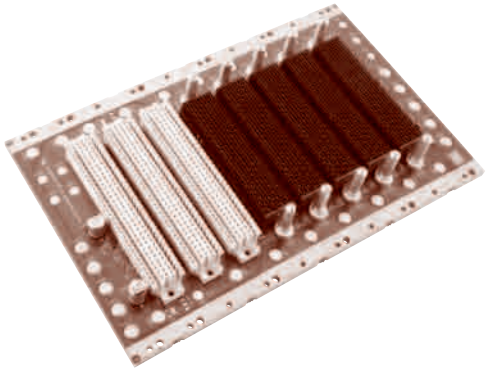
B18118232I	VXS 18 Slot + 2*Switch + 1*VME64x InfiniBand active
B18118242I	VXS 18 Slot + 2*Switch + 1*VME64x InfiniBand active with Rear I/O on VXS J0
B18118232R	VXS 18 Slot + 2*Switch + 1*VME64x Serial RapidIO active
B18118242R	VXS 18 Slot + 2*Switch + 1*VME64x Serial RapidIO active with Rear I/O on VXS J0
B18118233I	VXS 18 Slot + 2*Switch + 1*VME64x InfiniBand passive 3.3 V
B18118243I	VXS 18 Slot + 2*Switch + 1*VME64x InfiniBand passive 3.3 V with Rear I/O on VXS J0
B18118223R	VXS 18 Slot + 2*Switch + 1*VME64x Serial RapidIO passive 3.3 V
B18118243R	VXS 18 Slot + 2*Switch + 1*VME64x Serial RapidIO passive 3.3 V with Rear I/O on VXS J0
B18118235I	VXS 18 Slot + 2*Switch + 1*VME64x InfiniBand passive 5 V
B18118245I	VXS 18 Slot + 2*Switch + 1*VME64x InfiniBand passive 5 V with Rear I/O on VXS J0
B18118235R	VXS 18 Slot + 2*Switch + 1*VME64x Serial RapidIO passive 5 V
B18118245R	VXS 18 Slot + 2*Switch + 1*VME64x Serial RapidIO passive 5 V with Rear I/O on VXS J0

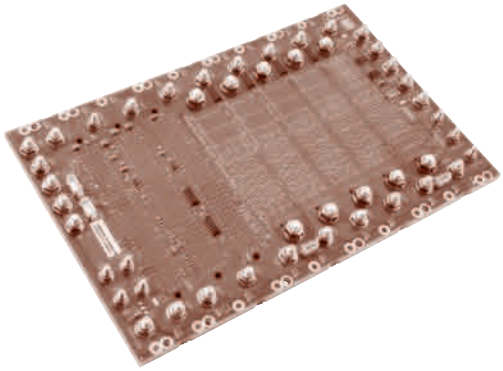
Switch Port to Payload Slot Channel Mapping (A+B) for these VXS-Backplanes (1 VME64x slot, 18 VXS slots and 2 switch slots):

Channel A/B	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Slot	10	13	9	8	14	15	7	6	16	17	5	4	18	19	3	2	20	21

VPX
3 U
Series 190







The VPXbus, based on ANSI/VITA 46.0 standard, is a new industrial standard for fast serial connections. The transmission rate is approximately 2.5 Gbps per lane (X1-Link).

For this hybrid-backplane an additional VMEbus signal mapping compliant with ANSI/VITA 46.1 is implemented. The connection to the approved VMEbus is done via VME64x-J1 slots.
ALL Hartmann VMEbus boards are based on the HIGH-SPEED DESIGN concept. Low reflection is achieved by means of uniform signal line surge impedance. Shielding of each individual signal line assures minimal coupling and therefore guarantees trouble-free operation.

Termination

In order to prevent interference on signal lines which might result from reflection at open line ends, these lines must be terminated on the VMEbus. A distinction is made between passive and active termination. The advantage of active termination is reduced closed-circuit current consumption. Passive termination features better frequency response.

Automatic daisy chaining

For this VPX-Backplane daisy chaining is implemented using an integrated OR logic. This logic closes the daisy chain when the daughter board is removed.

Chassis GND connection

There is a solid electrically conductive chassis GND surface in the backplane-to-card rack mounting area. This guarantees EMC-tight mounting of the bus board on the card rack.

HF coupling of card rack and system ground is implemented for VPX by capacitors (10 nF, 200 V in each slot). Static charges are discharged with a resistor (≥ 1 MΩ).

An additional Chassis-GND connection is provided with a M4 terminal screw.

Power connections

The main operating voltages and GND are supplied with M4 screw terminals. The auxiliary operating voltages are supplied via M3 screw terminals. Optimal daughter board supply and trouble-free operation are ensured by the arrangement of the feed modules on the backplane.

Standard VPX Slot Keying for 3 U Backplanes (Values in degree)

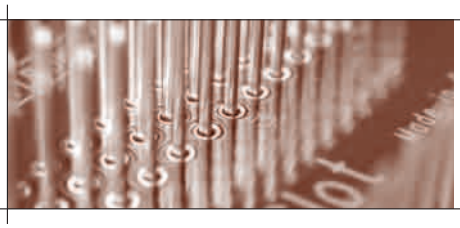
Slot	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
1	270	315	0	45	90	270	315	0	45	90	270	315	0	45	90	270	315	0	45	90	270
2	270	270	270	270	270	315	315	315	315	315	0	0	0	0	0	45	45	45	45	45	90

The standard orientation of coding keys is anytime changeable by the customer.
For backplanes made by Hartmann Electronic every key for every slot is settable to all 5 possible positions.

Utility connector

There are 2 connectors for system- management IPMB and SMB.

IPMB_PWR and SMB_PWR are connectable to power with 3-pin feed-through connectors (X2 and X4).
Usable voltages for IPMB are 5 V/3.3 V-AUX and for SMB 5 V/+5 V STBY.



JTAG-Stecker
In addition 2 JTAG-plugs for VPX-Slots 4 (X200) and 8 (X201) are available.

Jumper
Normally a battery voltage with approximately 3 V is available at Pin VBAT of connector VPX-J1. The voltage is externally accessible with connector X5 or internally using 3.3 V_AUX by closing jumper BR2.

If jumper BR1 is closed NVRMO is set to memory writeable.

System Controller Modul
The first VPX-Slot is provided for a system controller module. In this case jumper BR3 has to be closed.

Pin Assignments

Pin	IPMB (X1)	IPMB_PWR (X2)	SMB (X3)	SMB_PWR (X4)	JTAG (X200, X201)	VBAT (X5)	BR1	BR2	BR3
1	IPMB_SCL	+5 V	SMB_SCL	+5 V	GND	GND	NVMRO	+3.3 V_ AUX	SYS_CON*
2	GND	IPMB_PWR	GND	SMB_PWR	TCK	+3 V Batterie	GND	+ VBAT	GND
3	IPMB_SDA	+3.3 V_ AUX	SMB_SDA	+5 V STBY	TMS				
4	IPMB_PWR		SMB_PWR		TRST*				
5	NC		SMB_ ALERT		TDI				
6					TDO				

NC = not connected

Pin Assignments J0 VPX Utility Connector

Pin	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F	ROW G	ROW H	ROW I
1	VS2	VS2	VS2	VS2	None	VS1	VS1	VS1	VS1
2	VS2	VS2	VS2	VS2	None	VS1	VS1	VS1	VS1
3	VS3	VS3	VS3	VS3	None	VS3	VS3	VS3	VS3
4	GND	NVMRO	SYSRESET*	GND	-12 V_AUX	GND	SM3	SM2	GND
5	GND	SM1	SM0	GND	3.3 V_AUX	GND	GA4*	GAP*	GND
6	GND	GA0*	GA1*	GND	+12 V_AUX	GND	GA2*	GA3*	GND
7	TRST*	TMS	GND	GND	TDI	TDO	GND	GND	TCK
8	GND	GND	RES_BUS+	RES_BUS-	GND	GND	REF_CLK+	REF_CLK-	GND

VS1 = 12 V, VS2 = 3.3 V, VS3 = 5 V
* low-active

VPX
3 U
Series 190

Pin Assignments J1 VPX
Fabric for PXI Express - Fat Pipes x4

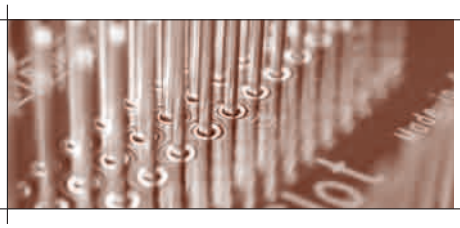
Pin	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F	ROW G	ROW H	ROW I
1	PA-RX0+	PA-RX0-	GND	GND	PA-TX0+	PA-TX0-	GND	GND	RESBUS_SE
2	GND	GND	PA-RX1+	PA-RX1-	GND	GND	PA-TX1+	PA-TX1-	GND
3	PA-RX2+	PA-RX2-	GND	GND	PA-TX2+	PA-TX2-	GND	GND	VBAT
4	GND	GND	PA-RX3+	PA-RX3-	GND	GND	PA-TX3+	PA-TX3-	GND
5	PB-RX0+	PB-RX0-	GND	GND	PB-TX0+	PB-TX0-	GND	GND	SYS_CON*
6	GND	GND	PB-RX1+	PB-RX1-	GND	GND	PB-TX1+	PB-TX1-	GND
7	PB-RX2+	PB-RX2-	GND	GND	PB-TX2+	PB-TX2-	GND	GND	REFCLK0_SE
8	GND	GND	PB-RX3+	PB-RX3-	GND	GND	PB-TX3+	PB-TX3-	GND
9	PC-RX0+	PC-RX0-	GND	GND	PC-TX0+	PC-TX0-	GND	GND	REFCLK1_SE
10	GND	GND	PC-RX1+	PC-RX1-	GND	GND	PC-TX1+	PC-TX1-	GND
11	PC-RX2+	PC-RX2-	GND	GND	PC-TX2+	PC-TX2-	GND	GND	REFCLK2_SE
12	GND	GND	PC-RX3+	PC-RX3-	GND	GND	PC-TX3+	PC-TX3-	GND
13	PD-RX0+	PD-RX0-	GND	GND	PD-TX0+	PD-TX0-	GND	GND	REFCLK3_SE
14	GND	GND	PD-RX1+	PD-RX1-	GND	GND	PD-TX1+	PD-TX1-	GND
15	PD-RX2+	PD-RX2-	GND	GND	PD-TX2+	PD-TX2-	GND	GND	SE7
16	GND	GND	PD-RX3+	PD-RX3-	GND	GND	PD-TX3+	PD-TX3-	GND

Pin Assignment on VPX J1 shows a 4x4 mapping (4 links with 4 lanes per link). This 5-slot VPX Backplane has a Full-Mesh topology.

Pin Assignments J2 VPX
VME on VPX, Single Ended

Pin	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F	ROW G	ROW H	ROW I
1	GND	D00	SYSFAIL*	GND	BBSY*	GND	ACFAIL*	D08	GND
2	GND	D01	BR0*	GND	BCLR*	GND	BG2IN*	D09	GND
3	GND	D02	BR1*	GND	BG0IN*	GND	BG2OUT*	D10	GND
4	GND	D03	BR2*	GND	BG0OUT*	GND	BG3IN*	D11	GND
5	GND	D04	BR3*	GND	BG1IN*	GND	BG3OUT*	D12	GND
6	GND	D05	AM0	GND	BG1OUT*	GND	BERR*	D13	GND
7	GND	D06	AM1	GND	SYSCLK	GND	LWORD*	D14	GND
8	GND	D07	AM2	GND	DS1*	GND	AM5	D15	GND
9	GND	AM4	AM3	GND	DS0*	GND	A23	A22	GND
10	GND	A07	IRQ7*	GND	WRITE*	GND	A21	A20	GND
11	GND	A06	IRQ6*	GND	DTACK*	GND	A19	A18	GND
12	GND	A05	IRQ5*	GND	AS*	GND	A17	A16	GND
13	GND	A04	IRQ4*	GND	IACK*	GND	A15	A14	GND
14	GND	A03	IRQ3*	GND	IACKIN*	GND	A13	A12	GND
15	GND	A02	IRQ2*	GND	IACKOUT*	GND	A11	A10	GND
16	GND	A01	IRQ1*	GND	RETRY*	GND	A09	A08	GND

* low-active



Pin Assignments J1 VME

Pin	ROW Z VME64x	ROW A VME	ROW B VME	ROW C VME	ROW D - Slot 1 VME64x	ROW D VME64x
1	MPR	D00	BBSY*	D08	VPC	VPC
2	GND	D01	BCLR*	D09	GND	GND
3	MCLK	D02	ACFAIL*	D10	+V1	+V1
4	GND	D03	BG0IN*	D11	+V2	+V2
5	MSD	D04	BG0OUT*	D12	RsvU-1	RsvU-1
6	GND	D05	BG1IN*	D13	-V1	-V1
7	MMD	D06	BG1OUT*	D14	-V2	-V2
8	GND	D07	BG2IN*	D15	RsvU-2	RsvU-2
9	MCTL	GND	BG2OUT*	GND	GAP*	GAP*
10	GND	SYSCLK	BG3IN*	SYSFAIL*	GA0*	GA0*
11	RESP*	GND	BG3OUT*	BERR*	GA1*	GA1*
12	GND	DS1*	BR0*	SYSRESET*	+3.3 V	+3.3 V
13	RsvBus1	DS0*	BR1*	LWORD*	GA2*	GA2*
14	GND	WRITE*	BR2*	AM5	+3.3 V	+3.3 V
15	RsvBus2	GND	BR3*	A23	GA3*	GA3*
16	GND	DTACK*	AM0	A22	+3.3 V	+3.3 V
17	RsvBus3	GND	AM1	A21	GA4*	GA4*
18	GND	AS*	AM2	A20	+3.3 V	+3.3 V
19	RsvBus4	GND	AM3	A19	SMB_SCL	RsvBus5
20	GND	IACK*	GND	A18	+3.3 V	+3.3 V
21	RsvBus6	IACKIN*	IPMB_SCL	A17	SMB_SDA	RsvBus7
22	GND	IACKOUT*	IPMB_SDA	A16	+3.3 V	+3.3 V
23	RsvBus8	AM4	GND	A15	SMB_ALERT*	RsvBus9
24	GND	A07	IRQ7*	A14	+3.3 V	+3.3 V
25	RsvBus10	A06	IRQ6*	A13	RsvBus11	RsvBus11
26	GND	A05	IRQ5*	A12	+3.3 V	+3.3 V
27	RsvBus12	A04	IRQ4*	A11	LI\I*	LI\I*
28	GND	A03	IRQ3*	A10	+3.3 V	+3.3 V
29	RsvBus13	A02	IRQ2*	A09	LI\O*	LI\O*
30	GND	A01	IRQ1*	A08	+3.3 V	+3.3 V
31	RsvBus14	-12 V	+5 V STDBY	+12 V	GND	GND
32	GND	+5 V	+5 V	+5 V	VPC	VPC

* low-active

Variation possibilities

These 5 terminations can be arbitrarily combined with one another:

VME	Systemmanagement 0+1	Systemmanagement 2+3	ReservedBus Differential	ReservedBus SingelEnded
Passive 3.3 V	IPMB	SingleEnded	SingleEnded	50 Ohm
Passive 5 V	SingleEnded	Differential	Differential	Not terminated
Active	Differential	Not terminated	Not terminated	
	Not terminated			

VPX
3 U, Series 190
Technical data

	VME64x J1	VPX J0, J1, J2
Base material	Fiberglass epoxide acc. to DIN 40802 (type FR408 or NE4000-13)	
Layer structure	Optimized for best HF behavior. Outer layers designed as shielding areas.	
Ohmic resistance of signal lines	< 1.0 Ω	
PCB thickness	4.3 mm	
Surge impedance Z of signal lines	60 Ω	100 Ω
Basic power consumption, both ends terminated	Active: < 0.1 A Passive: < 1.4 A	
• Power supply connection Screw-type terminal M3 and M4	X	
• Permissible current loading of a screw-type terminal M4	40 A	
• Permissible current loading of assembly per slot	at +3.3 V 15.0 A at +5 V 4.5 A at +12 V 1.5 A at –12 V 1.5 A at +V1 1.5 A at -V1 1.5 A at +V2 1.5 A at -V2 1.5 A at +5 V STDBY 1.5 A	at +3.3 V 22.0 A at +5 V 22.0 A at +12 V 22.0 A at +12 V_AUX 1.0 A at –12 V_AUX 1.0 A at +3.3 V_AUX 1.0 A
Installation height	3 HE/3 U	
Slot spacing	4 TE/4 HP	
Connectors	Press-fit quality class 2	
	160 pins IEC 61076-4-113	MultiGig RT2
Operating temperature range		
• Active termination	–40 °C ... +85 °C	
• Passive termination 3.3 V	–40 °C ... +85 °C	
• Passive termination 5V	–40 °C ... +70 °C	
Relative humidity	95 %, non-condensing	

	Order number
B190350230	VPX Bus 3xVMW 5xVPX terminated according to Variant 02: VME: passive 3.3 V terminated System management 0+1 IPMB System management 2+3: differential ReservedBusD: differential ReservedBusSE: 50 Ohm