6U OpenVPX BACKPLANE

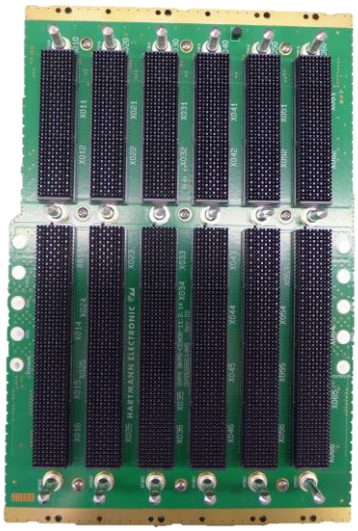
BKP6-CEN06-11.2.14-3

VITA 46
VITA 65

Key Features:

- Compliant to VITA 46.0 baseline specification
- Compliant to VITA 65 OpenVPX 6-CEN06-11.2.14-3
- 6 Slots VPX, 1 Payload Slot, 5 Peripheral Slots
- Configuration Data plane: Star (2xFP/Slot)
- M5 studs for power entry
- PCB size 261.85mm x 174,46mm x 5.4 mm
- 5 HP from slot to slot (25.40 mm)
- Flexible keying and alignment mechanism
- with geographical address pins
- System Management Interface on the backplane (I2CA, I2CB)
- with JTAG connector on first slot (JT1)
- Reference clock
- Auxilary clock
- Non-Volatile Memory Read Only signal set by Jumper BR1
- Battery backup option setting by Jumper XBAT. Vbat external or connected to 3.3 AUX.
- Max. Input current per backplane
  VS1/VS2:VS3 = 140A : 110A
- System Reset
- Operating temperature: -40° - +85°C
- Storage temperature: -55°C - +85°C
- Flammability rating: UL94-V0
- Custom assembly or modification on request

Front side



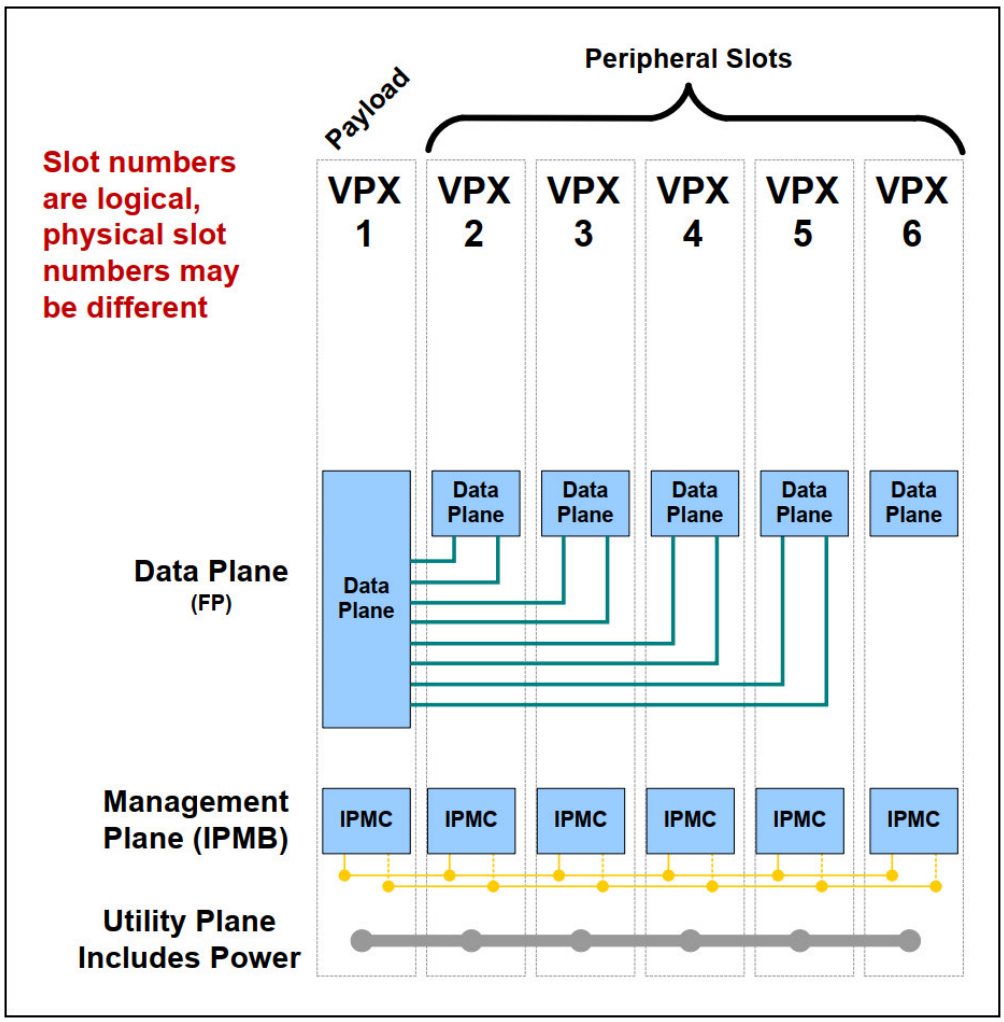
- **Order number: B196510960**

6U OpenVPX BACKPLANE **BKP6-CEN06-11.2.14-3**	**VITA 46** **VITA 65**	

1) Topology: 06-Slot — BKP6-CEN06-11.2.14-3 (1 Payload + 5 Peripheral)

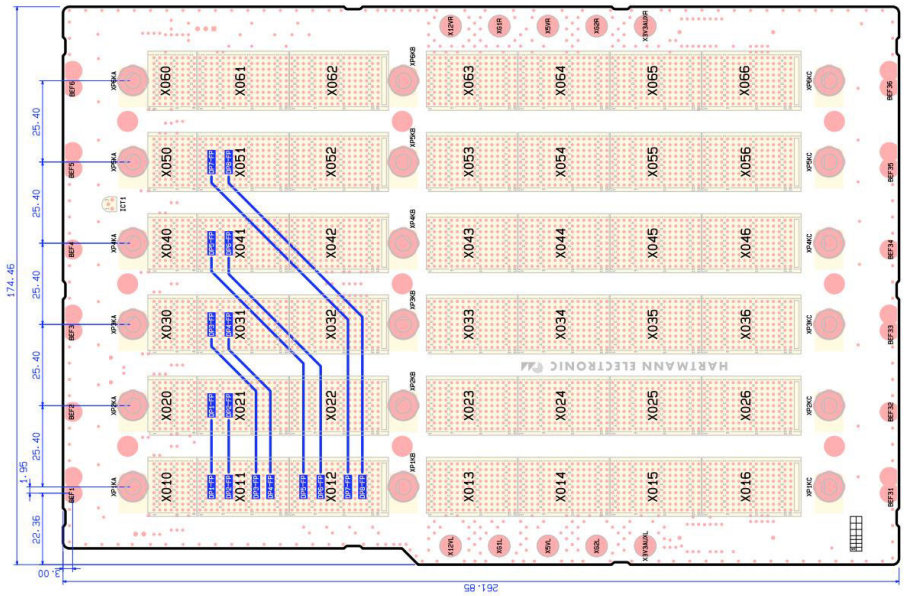
Profile Payload slot: SLT6-PAY-8F-10.2.3

Profile Peripheral slot: SLT6-PER-2F-10.3.2

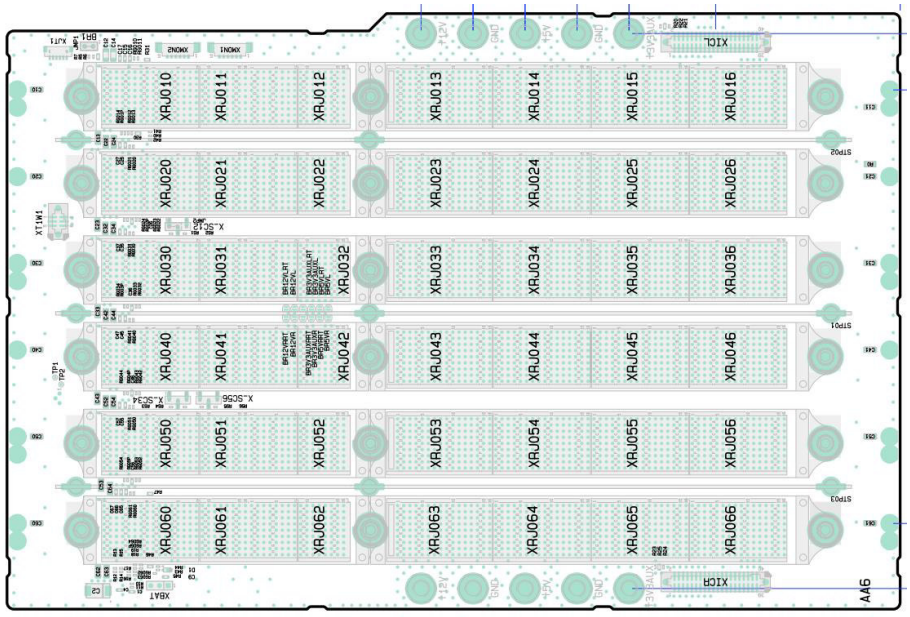


2) Drawings

Front Side



Rear Side



3) Pin Assignment

Pin Assignment VPX J0 (Utility Connector)

	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	No Pad*	Vs3	Vs3	Vs3
4	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1
6	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*
7	TCK	GND	TDO	TDI	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND

VS1=12V , VS2=12V , VS3=5V

Payload Slot Profile SLT6-PAY-8F-10.2.3— P1 & J1

Plug-In Module P1		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2		GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4		GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6		GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8		GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	Data Plane Port 3	UD	GND	GND-J1	DP03-T0-	DP03-T0+	GND	GND-J1	DP03-R0-	DP03-R0+
10		GND	DP03-T1-	DP03-T1+	GND-J1	GND	DP03-R1-	DP03-R1+	GND-J1	GND
11		UD	GND	GND-J1	DP03-T2-	DP03-T2+	GND	GND-J1	DP03-R2-	DP03-R2+
12		GND	DP03-T3-	DP03-T3+	GND-J1	GND	DP03-R3-	DP03-R3+	GND-J1	GND
13	Data Plane Port 4	UD	GND	GND-J1	DP04-T0-	DP04-T0+	GND	GND-J1	DP04-R0-	DP04-R0+
14		GND	DP04-T1-	DP04-T1+	GND-J1	GND	DP04-R1-	DP04-R1+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	DP04-T2-	DP04-T2+	GND	GND-J1	DP04-R2-	DP04-R2+
16		GND	DP04-T3-	DP04-T3+	GND-J1	GND	DP04-R3-	DP04-R3+	GND-J1	GND

6U OpenVPX BACKPLANE

BKP6-CEN06-11.2.14-3

VITA 46
VITA 65

Payload Slot Profile SLT6-PAY-8F-10.2.3— P2 & J2

Plug-In Module P2		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J2		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 5	UD	GND	*GND-J2*	DP05-T0-	DP05-T0+	GND	*GND-J2*	DP05-R0-	DP05-R0+
2		GND	DP05-T1-	DP05-T1+	*GND-J2*	GND	DP05-R1-	DP05-R1+	*GND-J2*	GND
3		UD	GND	*GND-J2*	DP05-T2-	DP05-T2+	GND	*GND-J2*	DP05-R2-	DP05-R2+
4		GND	DP05-T3-	DP05-T3+	*GND-J2*	GND	DP05-R3-	DP05-R3+	*GND-J2*	GND
5	Data Plane Port 6	UD	GND	*GND-J2*	DP06-T0-	DP06-T0+	GND	*GND-J2*	DP06-R0-	DP06-R0+
6		GND	DP06-T1-	DP06-T1+	*GND-J2*	GND	DP06-R1-	DP06-R1+	*GND-J2*	GND
7		UD	GND	*GND-J2*	DP06-T2-	DP06-T2+	GND	*GND-J2*	DP06-R2-	DP06-R2+
8		GND	DP06-T3-	DP06-T3+	*GND-J2*	GND	DP06-R3-	DP06-R3+	*GND-J2*	GND
9	Data Plane Port 7	UD	GND	*GND-J2*	DP07-T0-	DP07-T0+	GND	*GND-J2*	DP07-R0-	DP07-R0+
10		GND	DP07-T1-	DP07-T1+	*GND-J2*	GND	DP07-R1-	DP07-R1+	*GND-J2*	GND
11		UD	GND	*GND-J2*	DP07-T2-	DP07-T2+	GND	*GND-J2*	DP07-R2-	DP07-R2+
12		GND	DP07-T3-	DP07-T3+	*GND-J2*	GND	DP07-R3-	DP07-R3+	*GND-J2*	GND
13	Data Plane Port 8	UD	GND	*GND-J2*	DP08-T0-	DP08-T0+	GND	*GND-J2*	DP08-R0-	DP08-R0+
14		GND	DP08-T1-	DP08-T1+	*GND-J2*	GND	DP08-R1-	DP08-R1+	*GND-J2*	GND
15		UD	GND	*GND-J2*	DP08-T2-	DP08-T2+	GND	*GND-J2*	DP08-R2-	DP08-R2+
16		GND	DP08-T3-	DP08-T3+	*GND-J2*	GND	DP08-R3-	DP08-R3+	*GND-J2*	GND

Payload Slot Profile SLT6-PAY-8F-10.2.3— P3&J3

This connectors are all User Defined pins. See Section VITA65 6.3.3 for requirements and pin assignments concerning connectors that are all User Defined.

Backplane Jn	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	UD	UD	UD	UD	UD	GND	UD	UD	UD
2	GND	UD	UD	GND	UD	UD	UD	UD	GND
3	UD	UD	UD	UD	UD	GND	UD	UD	UD
4	GND	UD	UD	GND	UD	UD	UD	UD	GND
5	UD	UD	UD	UD	UD	GND	UD	UD	UD
6	GND	UD	UD	GND	UD	UD	UD	UD	GND
7	UD	UD	UD	UD	UD	GND	UD	UD	UD
8	GND	UD	UD	GND	UD	UD	UD	UD	GND
9	UD	UD	UD	UD	UD	GND	UD	UD	UD
10	GND	UD	UD	GND	UD	UD	UD	UD	GND
11	UD	UD	UD	UD	UD	GND	UD	UD	UD
12	GND	UD	UD	GND	UD	UD	UD	UD	GND
13	UD	UD	UD	UD	UD	GND	UD	UD	UD
14	GND	UD	UD	GND	UD	UD	UD	UD	GND
15	UD	UD	UD	UD	UD	GND	UD	UD	UD
16	GND	UD	UD	GND	UD	UD	UD	UD	GND

Payload Slot Profile SLT6-PAY-8F-10.2.3— P4 & J4

Plug-In Mod P4		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J4		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	User Defined	UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
2		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
3		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
4		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
5		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
6		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
7		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
8		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
9		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
10		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
11	RSVD	UD	GND	GND-J4	RSVD	RSVD	GND	GND-J4	RSVD	RSVD
12		GND	RSVD	RSVD	GND-J4	GND	RSVD	RSVD	GND-J4	GND
13	User Defined	UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
14		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
15		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
16		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND

Payload Slot Profile SLT6-PAY-8F-10.2.3— P5&J5-P6&J6

This connectors are all User Defined pins. See Section VITA65 6.3.3 for requirements and pin assignments concerning connectors that are all User Defined.

Backplane Jn	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	UD	UD	UD	UD	UD	GND	UD	UD	UD
2	GND	UD	UD	GND	UD	UD	UD	UD	GND
3	UD	UD	UD	UD	UD	GND	UD	UD	UD
4	GND	UD	UD	GND	UD	UD	UD	UD	GND
5	UD	UD	UD	UD	UD	GND	UD	UD	UD
6	GND	UD	UD	GND	UD	UD	UD	UD	GND
7	UD	UD	UD	UD	UD	GND	UD	UD	UD
8	GND	UD	UD	GND	UD	UD	UD	UD	GND
9	UD	UD	UD	UD	UD	GND	UD	UD	UD
10	GND	UD	UD	GND	UD	UD	UD	UD	GND
11	UD	UD	UD	UD	UD	GND	UD	UD	UD
12	GND	UD	UD	GND	UD	UD	UD	UD	GND
13	UD	UD	UD	UD	UD	GND	UD	UD	UD
14	GND	UD	UD	GND	UD	UD	UD	UD	GND
15	UD	UD	UD	UD	UD	GND	UD	UD	UD
16	GND	UD	UD	GND	UD	UD	UD	UD	GND

6U OpenVPX BACKPLANE

BKP6-CEN06-11.2.14-3

VITA 46
VITA 65

Peripheral Slot Profile SLT6-PER-2F-10.3.2 — P1 & J1

Plug-In Module P1		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	*GND-J1*	DP01-T0-	DP01-T0+	GND	*GND-J1*	DP01-R0-	DP01-R0+
2		GND	DP01-T1-	DP01-T1+	*GND-J1*	GND	DP01-R1-	DP01-R1+	*GND-J1*	GND
3		P1-VBAT	GND	*GND-J1*	DP01-T2-	DP01-T2+	GND	*GND-J1*	DP01-R2-	DP01-R2+
4		GND	DP01-T3-	DP01-T3+	*GND-J1*	GND	DP01-R3-	DP01-R3+	*GND-J1*	GND
5	Data Plane Port 2	SYS_CON*	GND	*GND-J1*	DP02-T0-	DP02-T0+	GND	*GND-J1*	DP02-R0-	DP02-R0+
6		GND	DP02-T1-	DP02-T1+	*GND-J1*	GND	DP02-R1-	DP02-R1+	*GND-J1*	GND
7		Reserved	GND	*GND-J1*	DP02-T2-	DP02-T2+	GND	*GND-J1*	DP02-R2-	DP02-R2+
8		GND	DP02-T3-	DP02-T3+	*GND-J1*	GND	DP02-R3-	DP02-R3+	*GND-J1*	GND
9	User Defined	UD	GND	*GND-J1*	UD	UD	GND	*GND-J1*	UD	UD
10		GND	UD	UD	*GND-J1*	GND	UD	UD	*GND-J1*	GND
11		UD	GND	*GND-J1*	UD	UD	GND	*GND-J1*	UD	UD
12		GND	UD	UD	*GND-J1*	GND	UD	UD	*GND-J1*	GND
13		UD	GND	*GND-J1*	UD	UD	GND	*GND-J1*	UD	UD
14		GND	UD	UD	*GND-J1*	GND	UD	UD	*GND-J1*	GND
15		Maskable Reset*	GND	*GND-J1*	UD	UD	GND	*GND-J1*	UD	UD
16		GND	UD	UD	*GND-J1*	GND	UD	UD	*GND-J1*	GND

Peripheral Slot Profile SLT6-PER-2F-10.3.2— P2&J2-P6&J6

This connectors are all User Defined pins. See Section VITA65 6.3.3 for requirements and pin assignments concerning connectors that are all User Defined.

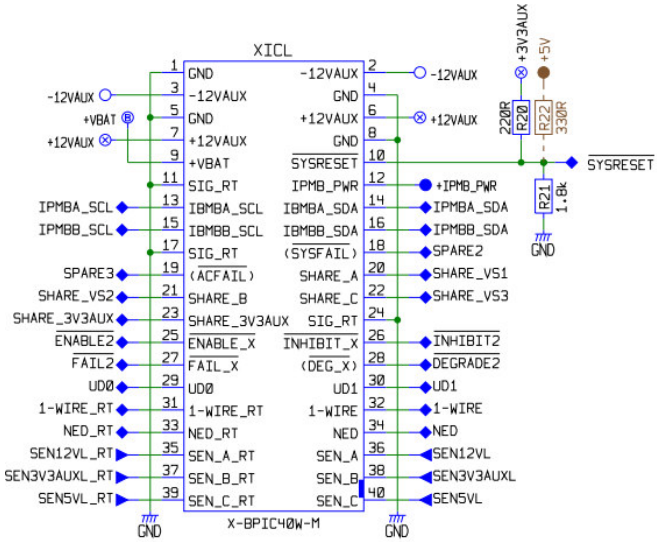
Backplane Jn	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	UD	UD	UD	UD	UD	GND	UD	UD	UD
2	GND	UD	UD	GND	UD	UD	UD	UD	GND
3	UD	UD	UD	UD	UD	GND	UD	UD	UD
4	GND	UD	UD	GND	UD	UD	UD	UD	GND
5	UD	UD	UD	UD	UD	GND	UD	UD	UD
6	GND	UD	UD	GND	UD	UD	UD	UD	GND
7	UD	UD	UD	UD	UD	GND	UD	UD	UD
8	GND	UD	UD	GND	UD	UD	UD	UD	GND
9	UD	UD	UD	UD	UD	GND	UD	UD	UD
10	GND	UD	UD	GND	UD	UD	UD	UD	GND
11	UD	UD	UD	UD	UD	GND	UD	UD	UD
12	GND	UD	UD	GND	UD	UD	UD	UD	GND
13	UD	UD	UD	UD	UD	GND	UD	UD	UD
14	GND	UD	UD	GND	UD	UD	UD	UD	GND
15	UD	UD	UD	UD	UD	GND	UD	UD	UD
16	GND	UD	UD	GND	UD	UD	UD	UD	GND

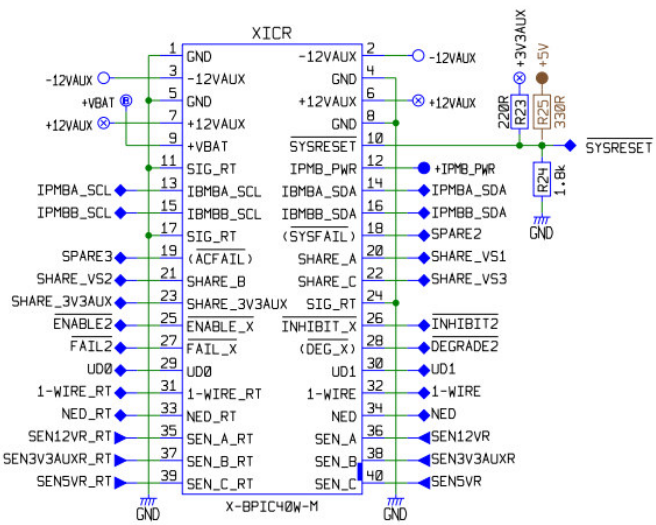
4) Current Capability:

+12V	140 A
+5V	110 A
-12V AUX	8 A
+12V AUX	8 A
+3.3V AUX	10 A

5) XICL and XICR Connector

There are two connector with the main control signals like sens, I2C, load sharing and auxiliary voltages on the Backplane.

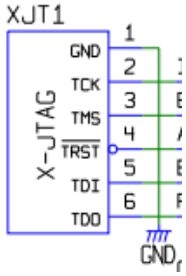




Connector Samtec TFM-120-02-S-D-WT

6) JTAG (connector XJT1)

For test and programming a JTAG connector (6-poles) is implemented (XJT1).



Connector JST
BM06B-SRSS-TBT(LF)(SN)

7) SYSCON

By setting the signal Syscon to GND the system slot is defined. In general the system slot is slot 1.

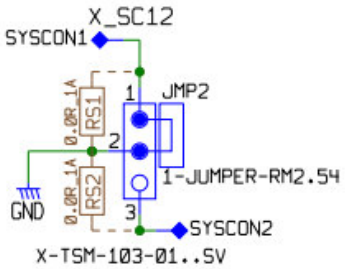
We offer 2 options for setting:

- Jumper (standard)

- 0 Ohm Resistor for rugged applications

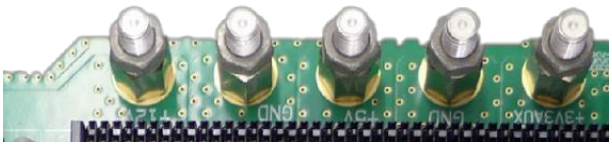
X_SC12

1	SYSCON1
2	GND
3	SYSCON2



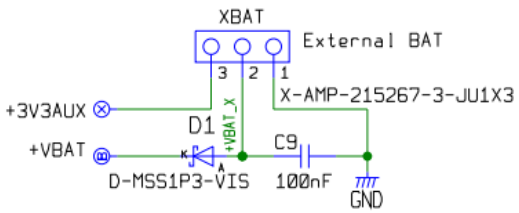
8) Power Studs M3

The main operating voltages (+12V, +3.3V, +5V) and GND are supplied with M3 screw terminals. The auxiliary operating voltages -12V Aux and +12V Aux are supplied via XICL and XICR.



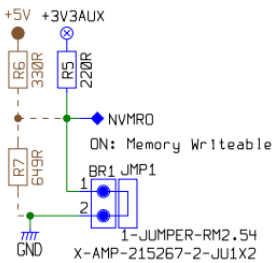
9) XBAT

Normally a battery voltage with approximately 3V is available at Pin VBAT of connector VPX-J1. The voltage is externally accessible with connector XBAT, Pin2 **or** internally using 3.3V_AUX by setting a Jumper between Pin2 and Pin3.



10) NVMRO

If Jumper BR1 is closed NVRMO is set to memory writeable.



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