


3U OpenVPX BACKPLANE with Coaxial Extension BKP3-DIS05-15.3.2-3

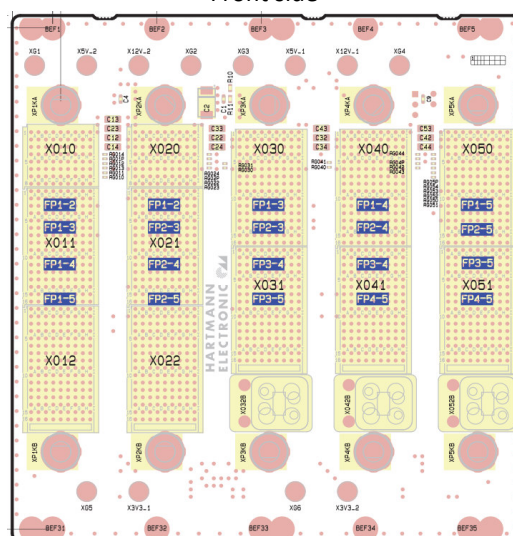
VITA 46
VITA 65
VITA 67.1



Key Features:

- Compliant to VITA 46.0 baseline specification
- Compliant to VITA 65 , BKP3-DIS05-15.3.2-3
- Compliant to VITA 67.1 Coaxial Interconnect On VPX
- 2+3 Slots VPX, 2 Payload Slots, 3 Payload Slots with coax
- Full Mesh X4 (4 Fat Pipes) configuration for Data Plane
- M3 studs for power entry
- PCB size 128.50 mm x 123.85 mm x 5.4 mm
- 5 HP from slot to slot (25.40 mm)
- Flexible keying and alignment mechanism
- with geographical address pins
- Reference clock
- Auxiliary clock
- System Reset
- With JTAG connector on first slot (JT1)
- System Management Interface on the backplane (I2CA, I2CB)
- Non-Volatile Memory Read Only signal set by Jumper BR1
- Battery backup option setting by Jumper XBAT. Vbat external or connected to 3.3 VAUX.
- Max. Input current per backplane
VS1:VS2:VS3 = 60A : 60A : 60A
- Operating temperature: -40°C - +85°C
- Storage temperature: -55°C - +85°C
- Flammability rating: UL94-V0
- Custom assembly or modification on request
- Order number: B193236760**

Front side



Back side



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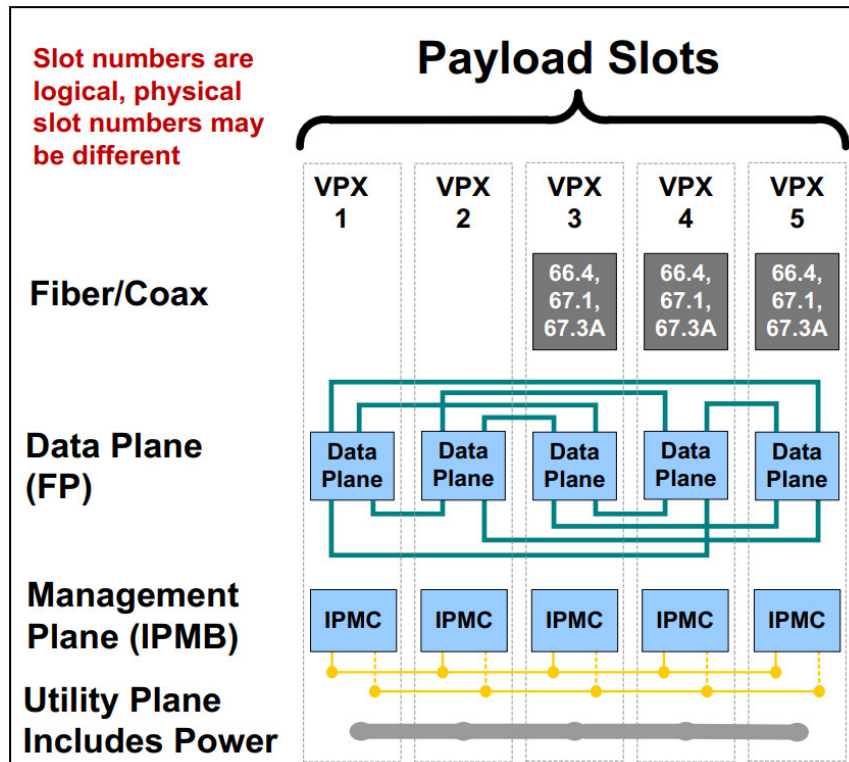
1) Topology: 5-Slot — BKP3-DIS05-15.3.2-3 (2 Payload + 3 Payload with coax)

Profile Payload slot without coax:

SLT3-SWH-4F-14.4.4 / MOD3-SWH-4F-16.4.5

Profile Payload slot with coax:

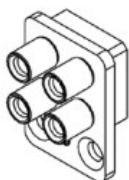
SLT3-PAY-4F1E-14.6.2 / MOD3-PAY-4F1E-16.6.2



2) Coaxial/RF Extension

This Backplane features VITA 67.1 RF Connector Modules in three of the slots.

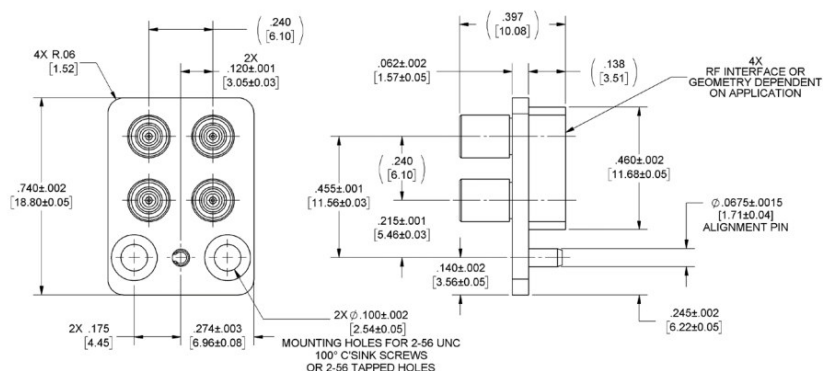
Coaxial Backplane Module by Tyco (item number 1996884-1)



DIMENSIONS ARE IN INCHES [mm]

ANGULAR: X" $\pm 1^{\circ}$
 X"X" $\pm 15^{\circ}$

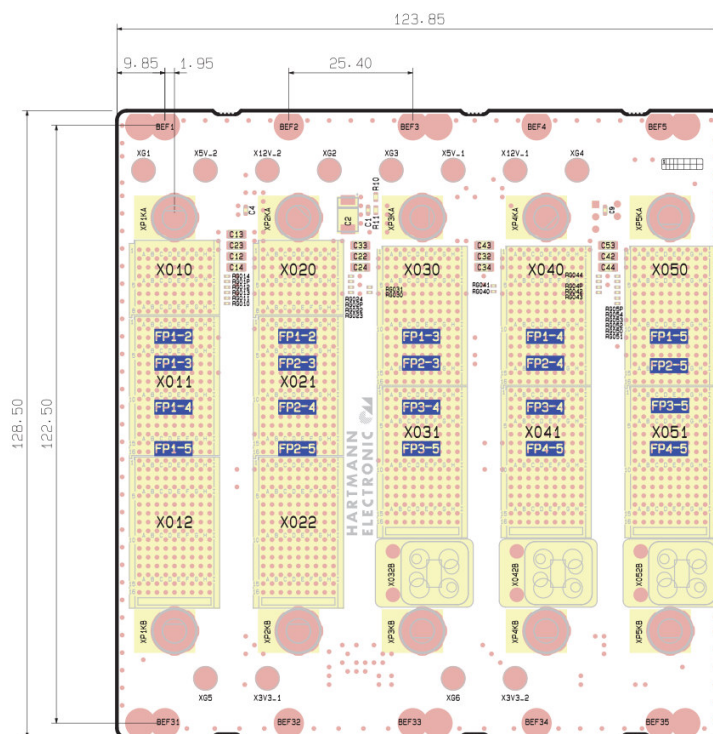
DECIMAL: X $\pm .030$
 .XX $\pm .010$
 .XXX $\pm .005$



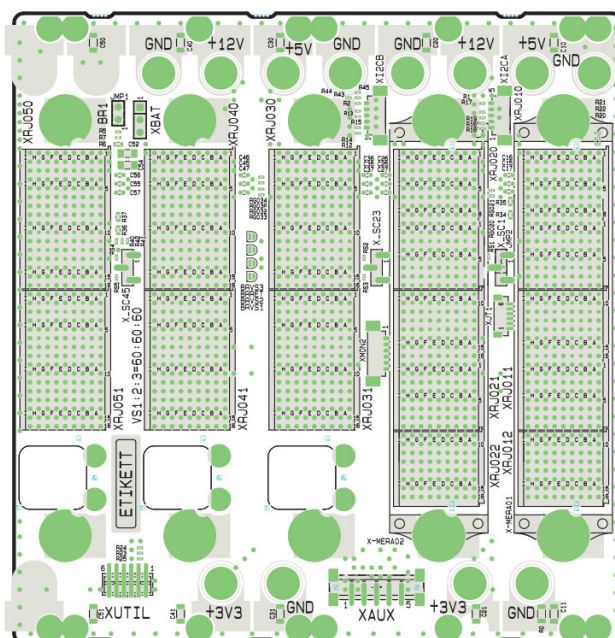
VITA 46
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Front side



Back side



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4) Pin Assignment

Pin Assignment VPX J0 (Utility Connector)

	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Vs1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad*	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

VS1=12V , VS2=3.3V , VS3=5V

Payload Slot Profile without coax SLT3-SWH-4F-14.4.4— P1 & J1

Plug-In Module P1		Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J1		Row i	Row h	Even	Odd	Row e	Row d	Even	Odd	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2		GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4		GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6		GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8		GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	Data Plane Port 3	UD	GND	GND-J1	DP03-T0-	DP03-T0+	GND	GND-J1	DP03-R0-	DP03-R0+
10		GND	DP03-T1-	DP03-T1+	GND-J1	GND	DP03-R1-	DP03-R1+	GND-J1	GND
11		UD	GND	GND-J1	DP03-T2-	DP03-T2+	GND	GND-J1	DP03-R2-	DP03-R2+
12		GND	DP03-T3-	DP03-T3+	GND-J1	GND	DP03-R3-	DP03-R3+	GND-J1	GND
13	Data Plane Port 4	UD	GND	GND-J1	DP04-T0-	DP04-T0+	GND	GND-J1	DP04-R0-	DP04-R0+
14		GND	DP04-T1-	DP04-T1+	GND-J1	GND	DP04-R1-	DP04-R1+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	DP04-T2-	DP04-T2+	GND	GND-J1	DP04-R2-	DP04-R2+
16		GND	DP04-T3-	DP04-T3+	GND-J1	GND	DP04-R3-	DP04-R3+	GND-J1	GND

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Payload Slot Profile without coax SLT3-SWH-4F-14.4.4— P2 & J2


This connector is all User Defined pins. See Section VITA 65 6.3.3 for requirements and pin assignments
Concerning connectors that are all User Defined.

Connector Example Combined Plug-In Module & Backplane - Differential

Backplane Jn	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	UD	UD	UD	UD	UD	GND	UD	UD	UD
2	GND	UD	UD	GND	UD	UD	UD	UD	GND
3	UD	UD	UD	UD	UD	GND	UD	UD	UD
4	GND	UD	UD	GND	UD	UD	UD	UD	GND
5	UD	UD	UD	UD	UD	GND	UD	UD	UD
6	GND	UD	UD	GND	UD	UD	UD	UD	GND
7	UD	UD	UD	UD	UD	GND	UD	UD	UD
8	GND	UD	UD	GND	UD	UD	UD	UD	GND
9	UD	UD	UD	UD	UD	GND	UD	UD	UD
10	GND	UD	UD	GND	UD	UD	UD	UD	GND
11	UD	UD	UD	UD	UD	GND	UD	UD	UD
12	GND	UD	UD	GND	UD	UD	UD	UD	GND
13	UD	UD	UD	UD	UD	GND	UD	UD	UD
14	GND	UD	UD	GND	UD	UD	UD	UD	GND
15	UD	UD	UD	UD	UD	GND	UD	UD	UD
16	GND	UD	UD	GND	UD	UD	UD	UD	GND

Payload Slot Profile with coax SLT3-PAY-4F1E-14.6.2— P1 & J1

Plug-In Module P1	Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J1	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2	GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3	P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4	GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6	GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7	Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8	GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	UD	GND	GND-J1	DP03-T0-	DP03-T0+	GND	GND-J1	DP03-R0-	DP03-R0+
10	GND	DP03-T1-	DP03-T1+	GND-J1	GND	DP03-R1-	DP03-R1+	GND-J1	GND
11	UD	GND	GND-J1	DP03-T2-	DP03-T2+	GND	GND-J1	DP03-R2-	DP03-R2+
12	GND	DP03-T3-	DP03-T3+	GND-J1	GND	DP03-R3-	DP03-R3+	GND-J1	GND
13	UD	GND	GND-J1	DP04-T0-	DP04-T0+	GND	GND-J1	DP04-R0-	DP04-R0+
14	GND	DP04-T1-	DP04-T1+	GND-J1	GND	DP04-R1-	DP04-R1+	GND-J1	GND
15	Maskable Reset*	GND	GND-J1	DP04-T2-	DP04-T2+	GND	GND-J1	DP04-R2-	DP04-R2+
16	GND	DP04-T3-	DP04-T3+	GND-J1	GND	DP04-R3-	DP04-R3+	GND-J1	GND

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Payload Slot Profile with coax SLT3-PAY-4F1E-14.6.2— P2 & J2

This connector is only a half-connector (wafers 1 to 0). It is all User Defined pins. See

VITA 65.0 Section 6.3.3 for requirements and pin assignments

Concerning connectors that are all User Defined.

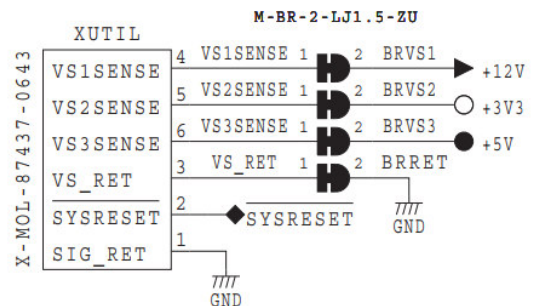
Connector Example Combined Plug-In Module & Backplane - Differential

Backplane Jn	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	UD	UD	UD	UD	UD	GND	UD	UD	UD
2	GND	UD	UD	GND	UD	UD	UD	UD	GND
3	UD	UD	UD	UD	UD	GND	UD	UD	UD
4	GND	UD	UD	GND	UD	UD	UD	UD	GND
5	UD	UD	UD	UD	UD	GND	UD	UD	UD
6	GND	UD	UD	GND	UD	UD	UD	UD	GND
7	UD	UD	UD	UD	UD	GND	UD	UD	UD
8	GND	UD	UD	GND	UD	UD	UD	UD	GND
9	UD	UD	UD	UD	UD	GND	UD	UD	UD
10	GND	UD	UD	GND	UD	UD	UD	UD	GND
11	UD	UD	UD	UD	UD	GND	UD	UD	UD
12	GND	UD	UD	GND	UD	UD	UD	UD	GND
13	UD	UD	UD	UD	UD	GND	UD	UD	UD
14	GND	UD	UD	GND	UD	UD	UD	UD	GND
15	UD	UD	UD	UD	UD	GND	UD	UD	UD
16	GND	UD	UD	GND	UD	UD	UD	UD	GND

5) Current Capability:

▪ +12V	60 A
▪ +3.3V	60 A
▪ +5V	60 A
▪ -12V AUX	5 A
▪ +12V AUX	5 A
▪ +3.3V AUX	5 A

6) UTILITY (Connector XUTIL)



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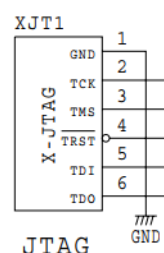
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7) JTAG (Connector XJT1)



Consider: JTAG only at Slot 1, Payload slot



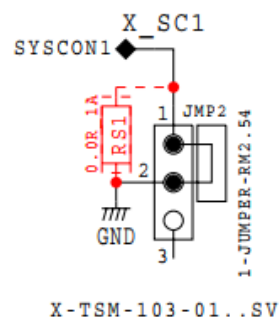
8) SYSCON

By setting the signal Syscon to GND the system slot is defined. In general the system slot is slot 1.

There are additional connectors X_SC23 and X_SC45 so as you can select any slot as system slot

X_SC12

1	SYSCON1
2	GND
3	SYSCON2



We offer 2 options for setting:

- Jumper (standard)
- 0 Ohm Resistor for rugged applications

9) I2C Connector

There are 2 connectors for system-management I2CA and I2CB.

For customer specific board assembly Zero-Ohm resistors available.

Usable voltages for I2C are 3.3V-AUX

I2CA

1	I2CA_SCL
2	GND
3	I2CA_SDA
4	I2CA_PWR
5	NC

I2CB

1	I2CB_SCL
2	GND
3	I2CB_SDA
4	I2CB_PWR
5	NC

**3U OpenVPX BACKPLANE
with Coaxial Extension**
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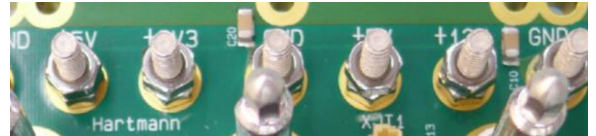
**VITA 46
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10) Power Connections via M3 studs

The main operating voltages and GND are supplied with M3 studs.

The auxiliary operating voltages are supplied via 5 pole plug connector. Optimal daughter board supply and trouble-free operation are ensured by the arrangement of the feed modules on the backplane.

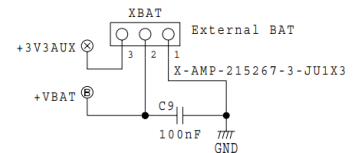


11) XBAT

Normally a battery voltage with approximately 3V is available at Pin VBAT of connector VPX-J1. The voltage is externally accessible with connector XBAT, Pin2 or internally using 3.3V_AUX by setting a Jumper between Pin2 and Pin3.

XBAT

1	GND
2	+VBAT
3	+3.3V_AUX

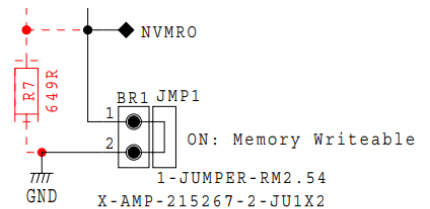


12) NVMRO

If Jumper BR1 is closed NVRMO is set to memory writeable.

BR1

1	NVMRO
2	GND



Germany

Hartmann Electronic GmbH
Phone: +49 711 13 98 90
Fax: +49 711 8 66 11 91
vertrieb.he@kontron.com
www.hartmann-electronic.com

USA

Kontron
Fabian Hemmann
Phone: +1 937-324-2420
Mobile: +1 937 346 7878
fabian.hemmann@us.kontron.com
www.hartmann-electronic.com

France

Kontron Modular Computers S.A.S.
Serge Pichat
Phone: +33 (0)9 66 44 03 15
Mobile: +33 (0)6 82 62 16 00
Serge.pichat@kontron.com
www.hartmann-electronic.com

India

Hartmann Electronic GmbH
Vivek Deshpande
Phone: +1 91 20 66 74 51 23
Vivek.Deshpande@kontron.com
www.hartmann-electronic.com