# PXIe Backplane

# PXIe 3U 8 Slot series backplane

# User Manual

# Revision History

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Hartmann Electronic is a longstanding partner of the embedded industry and has a variety of different backplanes. With our wide selection of backplanes and enclosure you can build your perfect system platform

# Content

# 1. Safety

## *Intended application*

PXI Express PXCe1008 series backplane are not end-products with independent functionality according to the EMC regulations, an operational system is achieved only by combining the backplane with appropriate plug-in PCI/PXIe instruments. As a consequence, formal certification requirements as for instance the CE marking do not apply to it.

The completion and final testing of the units has to be carried out, or at least supervised, by a qualified technician. The following instructions are directed exclusively to this qualified personal, i.e. engineers, trained and qualified electricians etc.

Make sure that the finished system complies with the safety regulations currently applicable in the country in which it will be used.

## *Safety symbols*

| | |
|---|---|
|  | **Hazardous voltage!**<br>*Familiarize yourself with the danger of electrical voltages and the safety precautions before starting to work with parts that carry dangerous voltages* |

| | |
|---|---|
|  | **Caution!**<br>*This symbol indicates a condition where damage of the equipment or injury of the service personnel could occur. To reduce the risk of damage or injury, follow all steps or procedures as instructed.* |

| | |
|---|---|
|  | **Danger of electrostatic discharge!**<br>*Static electricity can damage sensitive components in a system. To avoid damage, wear ESD wrist straps or at regular intervals touch blank enclosure parts.* |

## *General safety precautions*

| | |
|---|---|
|  | **Warning!**<br>*Voltages over 60 VDC can be present in this equipment. This equipment is intended to be accessed, to be installed and maintained by qualified and trained service personnel only.*<br>*This equipment is designed in accordance with protection class 1!*<br>*It must therefore be operated only with protective GND/earth connection!* |

# *Safety instructions*

The intended audience of this User Manual are system Integrators and hardware/software engineers.

The product has been designed to meet relevant standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control. It shall not be used in safety-critical applications, life-sustaining appliances or in aircrafts.

Only trained personnel or persons qualified in electronics or electrical engineering are authorized to install, operate or maintain the product.

This section provides safety information about:

- Protection Against Electromagnetic Interference (EMI)
- Electrostatic Discharge Precautions
- System Installation

## Protection against electromagnetic interference (EMI)

The product has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules, EN 55022 Class A.

To ensure proper EMC shielding, operate the custom chassis only with all free slots populated with filler panels.

Ensure that all EMI gaskets make correct contact.

## Electrostatic discharge precautions

Electronic components can easily be destroyed by electrostatic discharge which can occur between backplane components and a person.

- Before working on the backplane make sure that you are working in an ESD-safe environment.

## Installation

To avoid backplane damage, verify that the system environment meets the environmental and power requirements given in this guide before installation consider these guidelines:

## Location

Locate the system in a stable area free of excessive movement and jarring, dust, smoke, and electrostatic discharge (ESD). Make sure that the temperature does not exceed the operating temperature given in the environmental requirements in this guide and allow room for proper air flow for cooling.

## Voltage hazards

The system is powered with a power supply the mains voltage is 115/230VAC.
(Voltage range 90VAC to 264VAC)

This voltage is considered hazardous.

## System overheating

Ensure clearance of at least 10 cm to the air inlet on the left side of the backplane, and a free path of at least 10 cm for the air exhaust on the right.
Shelf ambient temperature may not exceed 50°C.

## Mounting considerations

During the course of handling, shipping, and assembly, parts could become loose or damaged. Do not operate a shelf in this condition, as this may cause damage to other equipment.

## Electrical hazards

The caution label on the system's rear near the grounding studs shows that you have to create an earth connection because there may be a high leakage current which is considered hazardous.

High leakage current can cause injuries.
Ensure that the system is properly grounded at all times, the following conditions shall be met:

- This equipment shall be connected directly to the AC supply system earth ground

# 2. Product description

The PXIe 3U series Backplane is an 8 Slot PXI Express Backplane. The Backplane fully complies with the *PXI-5 PXI Express Hardware Specification*.
There is one PXIe system Slot, one PXIe peripheral slot, 2 fully Hybrid peripheral slots and 4 PXI legacy slots available on the backplane.

The key features of the PXIe 3U series Backplane is Backplane include the following:

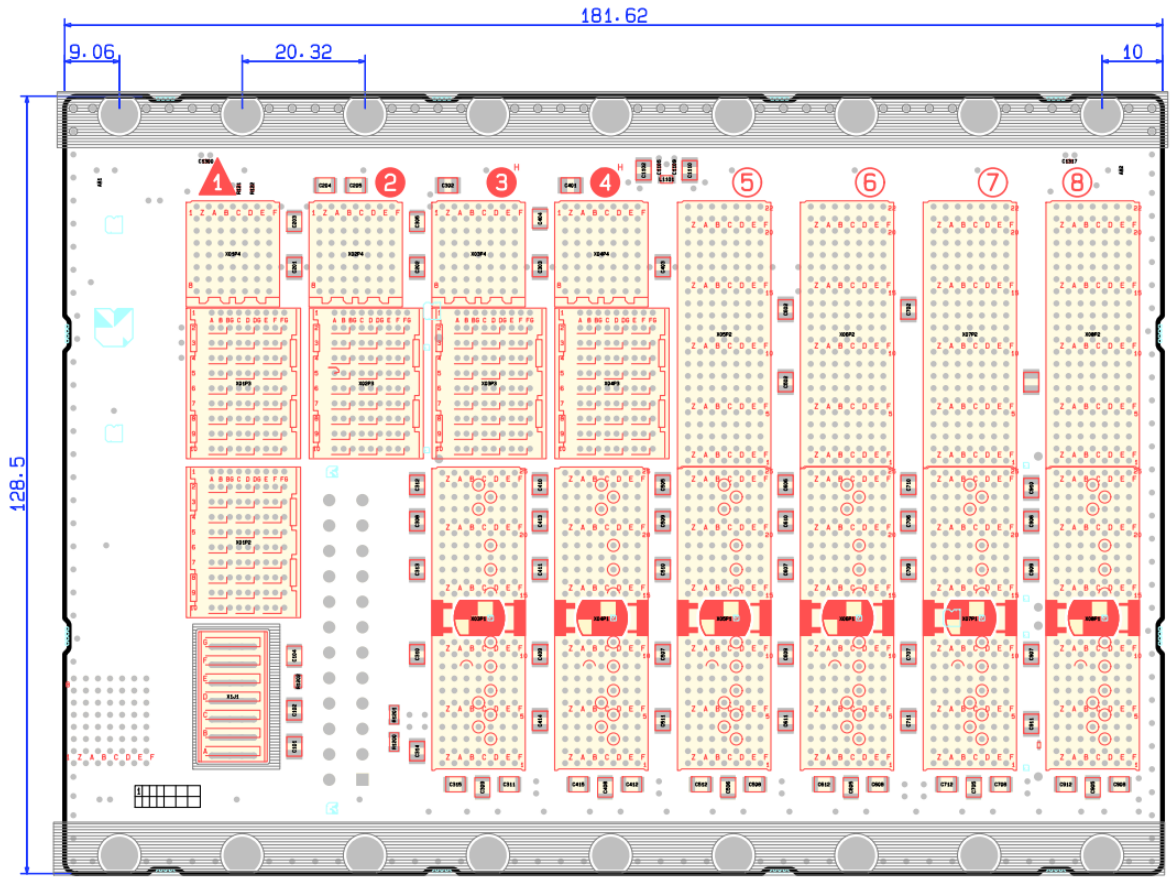
- Rear Panel PXI_CLK10 I/O Connector
- Complies with PXI and CompactPCI Specification
- 0-50°C Temperature Range
- On/Standby momentary power switch on the front panel for easy use
- Low jitter PXI Express Clocks with 25 ppm stability
- Software multi-vendor interoperability
- Module multi-vendor interoperability
- 24 pin ATX Power input connector

## *Related documentation*

- *PXI-5 PXI Express Hardware Specification*
- CompactPCI PICMG 2.0 R. 3.0
- *CompactPCI Express Specification PICMG EXP.0 Revision 2.0*

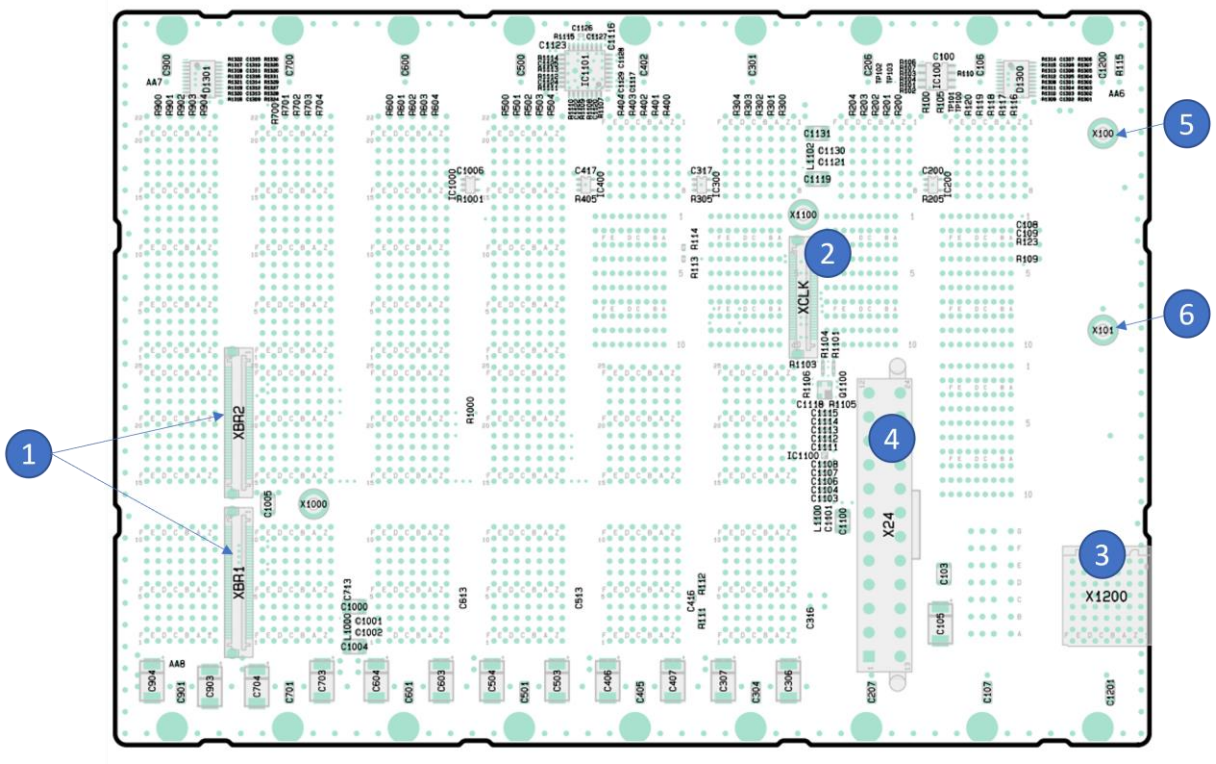
# *Backplane description*

Figure 2-1 Front view of the PXIe 3U 8 Slot Series Backplane




PXIe system slot 1
PXIe peripheral slot 2
PXIe hybrid slots 3,4
PXI Legacy slots 5,6,7,8

Figure 2-2 Rear view of the PXIe 3U 8 Slot Series Backplane




1 Bridge module connector (XBR1, XBR2)
2 Clock module connector (XCLK)
3 Chassis management interface connector
4 24 Pin ATX Power Connector
5 X100 „PWR_BTN#“; M2 internal thread
6 X101 „RTN_PWR_BTN#“, M2 internal thread

## System controller slot

The system Controller slot 1 of the backplane is a 4-Link configuration system slot as defined in the CompactPCI Express and PXI Express Specification.
The backplane connects the system slot using three PCIe X4 links to the peripheral slots. One PCIe link of the system slot connects to a PCIe Switch using PCIe Gen 2 X1. The PCIe to PCI bridge provides PCI connection to the PXIe hybrid slots and the PXI legacy slots.
The PXIe hybrid slots 3 and 4 are connected to the PCI Bus. The PCIe- to PCI bridge provides a 32-bit, 33Mhz PCI Bus.
In order to support higher data rates on the PCI bus ask Hartmann Electronic to configure the PCI bus for 32-bit, 66 Mhz operation according to cPCI specification.
The system controller slot has also connectivity to PXI_CLK10, PXI Trigger Bus and PXI Local Bus 6.
The mechanical momentary switch at the front panel transitions the PWRBTN# from open-circuit to GND to open circuit. The system board uses this ON/OFF state to control the PS_ON# signal. The PS_ON# signal turns on the backplane' main power supply.

## PXIe peripheral slot

The backplane provides one PXIe peripheral slot. The peripheral slot is fully compliant with the *PXI-5 PXI Express Hardware Specification*. The backplane connects the System slot using PCIE Gen2 X4 to the PXIe peripheral slot. The PXI Express peripheral slot can accept the following modules:

- A PXI Express peripheral module.
- A PXI Express hybrid peripheral module.
- A CompactPCI Express Type-2 Peripheral module.
- A CompactPCI 32-bit peripheral with +5 V V(I/O).

## PXIe hybrid peripheral Slots

The PXIe 3U 8 slot backplane provides 2 PXIe hybrid peripheral slots that are fully compliant with the *PXI-5 PXI Express Hardware Specification.* The PXI Express hybrid peripheral slots can accept the following modules:

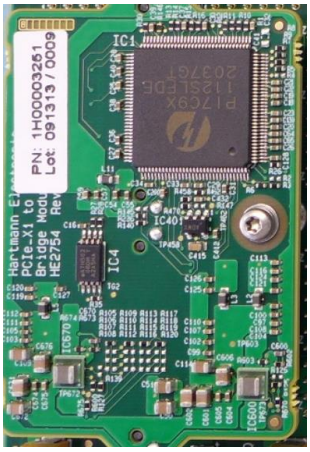
- A PXI Express peripheral module.
- A CompactPCI Express Type-2 Peripheral module.
- A hybrid-compatible PXI peripheral module that has been modified by replacing the J2 connector with an XJ4 connector installed in the upper eight rows of J2. Refer to PXI Express specification for details. The PXI peripheral communicates through the backplane's 32-bit PCI bus.

## 24 pin ATX power Input connector

To provide power input into the backplane, the backplane is equipped with a 24 Pin ATX power connector, which is fully compliant to the ATX specification.

## *PCIe to PCI bridge module*

The backplane features a PCIe to PCI bridge Module which translates the serial PCIe bus into the parallel PCI bus. The PCI bus is needed for the connection to legacy PXI slots and devices. In order to support legacy PXI slots as well as PXI Express fully Hybrid slots the PCIe-PCI Bridge Module is plugged between two device slots at the rear side of the backplane.




**Featuring Diodes Inc Bridge PI7C9X112SLFDE**

The bridge Module is optimized for transfers from burst capable PCI Bus masters. The Module supports 32 bit 33 MHz operation as well as 32 bit 66 MHz operation.

## *PXIe clock module*

The Hartmann Electronic PXI Express Clock Module generates clocks, according to the PXI Express Hardware Specification, for the synchronization of PXI Express slot cards.


**Featuring 500MHz quartz oscillator**

The PXI Express clocks are synchronized to an internal or external high accurate 10 MHz clock source. As soon as an external clock source is available, the VCXO-based module, automatically synchronizes to the external source. The switching between the clock sources is realized through automatic retrieve switchover. That allows the PXI Express Chassis user to glitch free hot plug an external clock source to a running system.

## *Chassis management interface*

(Not scope of delivery, see ordering information)

Hartmann Electronic PXI Express Backplanes provide the ability of expanding the Chassis Management functions with the use of a custom specific PXIe Rear Module. This Module can be plugged into a connector at the rear side of the backplane shown in figure 2-2.

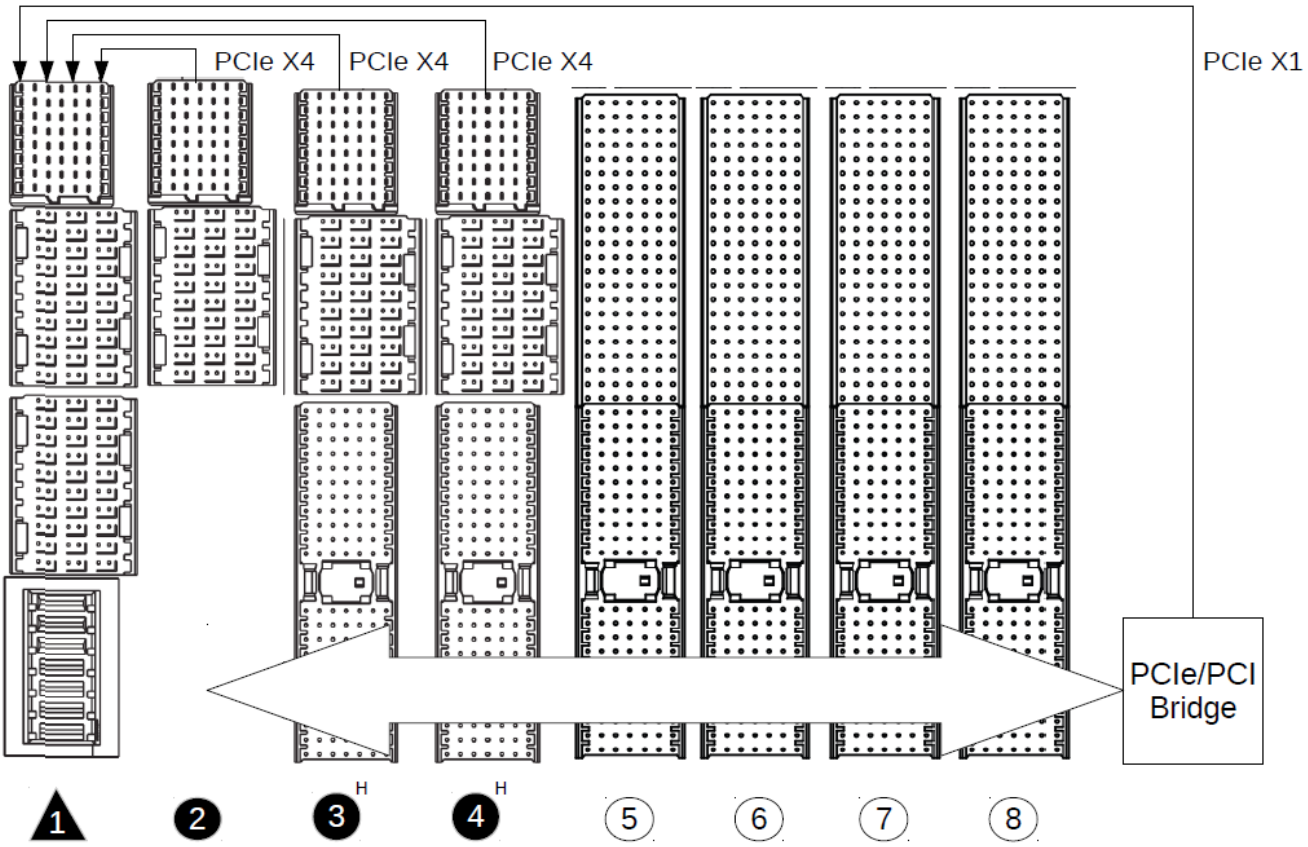
The custom PXIe rear module can be equipped with various functions:

- PXI Star Trigger I/Os
- PXI(e) timing and synchronization input and output clocks
- Fan control, power On control
- Reset control, DB-9 power monitor connector

Contact Hartmann Electronic for further information.

## PCI Express backplane diagram

Figure 2-4 shows the PXIe 3U 8slot series backplane's PCIe interface.




Slots 2, 3 and 4 are connected to the system slot using PCIe X4. These slots have up to 2 GB/s (single direction) dedicated bandwidth (X4 Gen-2 PCI Express).
Slots 5 and 8 are connected to the system by a PCIe to PCI bridge.

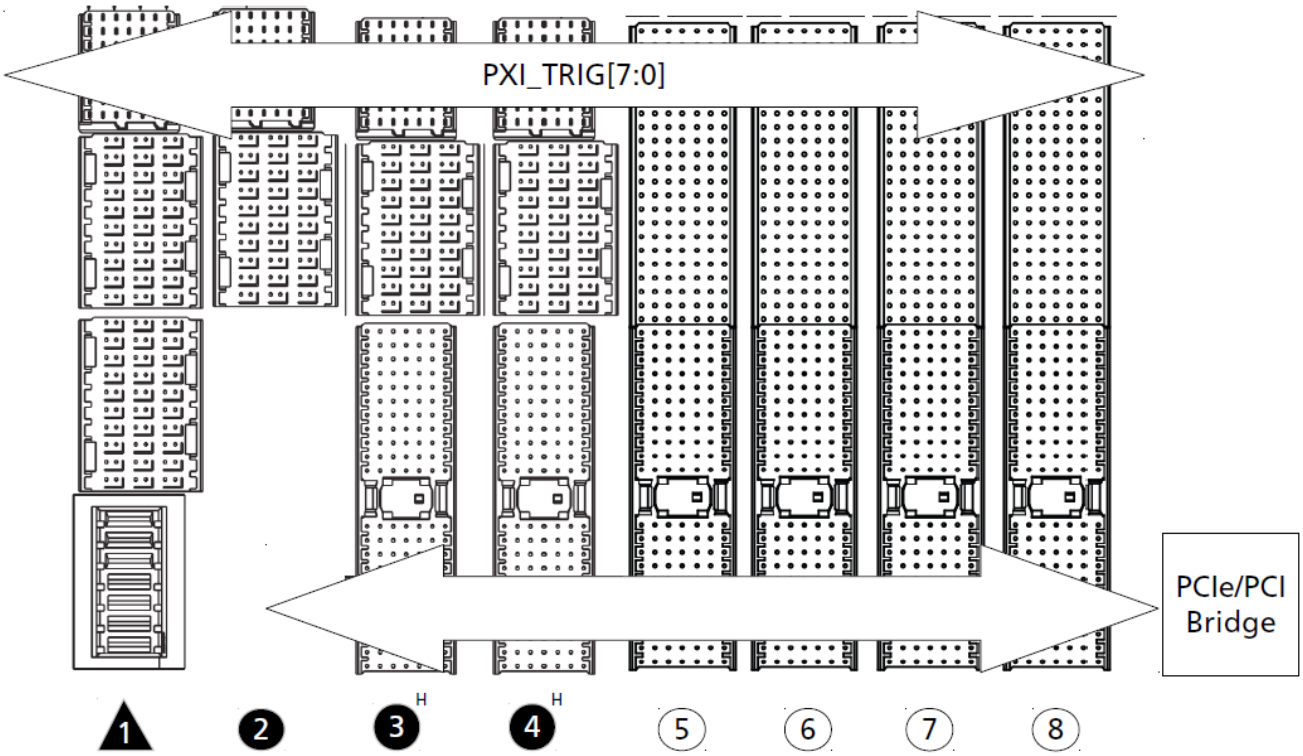
## PXI Local bus

The PXIe backplane local bus is a daisy-chained bus, that connects each peripheral slot with adjacent peripheral slots to the left and right.
The backplane routes PXI Local Bus 6 between all slots. The left Local Bus 6 from Slot 1 is not routed anywhere and the right local bus signal from slot 8 is not routed anywhere.
Local bus signals may range from high-speed TTL signals to analog signals as high as 42 V.

## *PXI Trigger bus*

All slots share eight trigger lines.

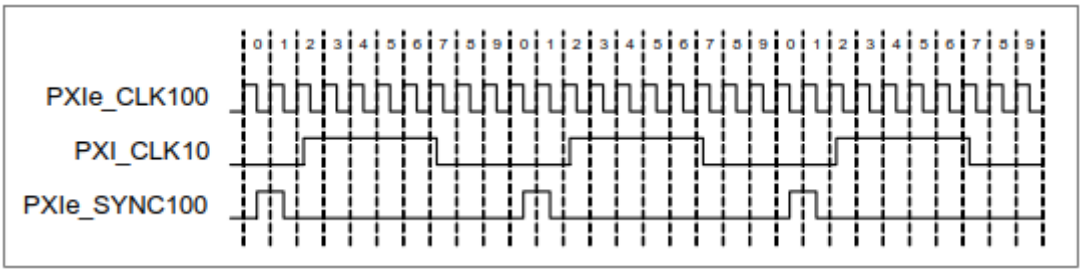
Figure 2-5 shows the PXIe 3U 8slot series backplane's Trigger interface.



## *System reference clock*

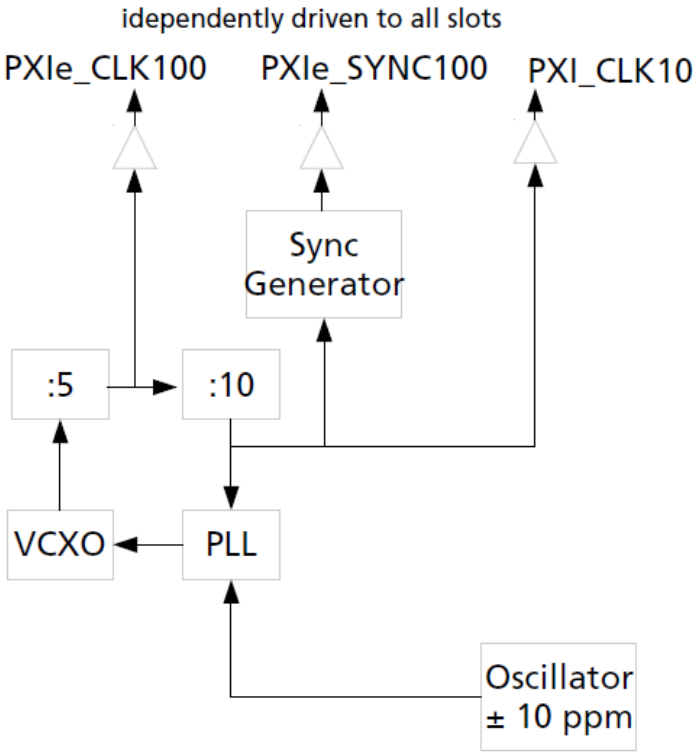
The PXIe 3U 8slot series backplane supplies PXI_CLK10, PXIE_CLK100, and PXIE_SYNC100 independently driven to each slot.
PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 have the default timing relationship according to *PXI-5 PXI Express Hardware Specification.*

The timing relations are as shown in Figure 2-6.




The 10 MHz reference clock input is derived from an internal clock oscillator.

Figure 2-7 shows the Clock architecture of the PXIe 3U 8slot series backplane.




The PLL is connected to the 10ppm 10 MHz clock oscillator. All clock outputs are synchronous to the 10 MHz reference clock input through the oscillator.

Each of the clocks PXI_CLK10, PXIE_CLK100, and PXIE_SYNC100 are driven with independent buffers.

## *Interoperability with CompactPCI*

The PXIe 3U 8slot series backplane allows you to flexibly use the following devices in a single PXI Express system:

- PXI Express compatible products
- CompactPCI Express compatible Type-2 peripheral products
- PXI hybrid slot compatible products
- Standard CompactPCI peripheral products

The PCI Clock has a frequency of 33 MHz. Therefore, the M66EN Pin of the CompactPCI bus is pulled down to Ground at the backplane. Removing the pull down resistor will enable the 32 bit, 66 Mhz operation on the PCI bus.
Ask Hartmann Electronic for further information on 66 MHz PCI bus signaling.

# 3. Installation

## *Connecting backplane chassis ground*

The backplane has a gold plated mounting area at the front side. The gold plated area must conduct to the chassis' extruded profiles in order to conduct the chassis to the chassis ground potential.

The backplane must be screwed to the extruded profiles from the rear side of the chassis.

It is strictly recommended to tighten the backplane to the extruded profiles with a screw, for each available backplane mounting hole. That will increase the EMI performance of the Custom PXI Express System.

## *Inspecting the backplane components*

During the course of handling, shipping, and assembly, pins, shrouds, mounting screws, and other items can become damaged and/or loose.

**WARNING:** Before utilizing the backplane, perform a thorough inspection to ensure the backplane and its components are not damaged.

- To inspect the backplane:

1. Visually inspect the backplane to ensure that all of the connector pins are straight, screws are tight, and so on.

## *Installing hardware*

The backplane is designed according to the 19” sub rack specification.
Care must be taken with the integration of the backplane into a third party chassis.
Follow the instructions of your system integrator in order to develop a chassis according to the effective specifications.

# Service

## Technical support and return for service assistance

Please return the complete backplane system. For all product returns and support issues, please contact your Hartmann sales distributor or www.hartmann-electronic.com

Please use the original packing material. Shipping without the original packing material might void the warranty.

## Declaration of conformity

The HARTMANN PXIe 3U 8slot series backplanes are developed and manufactured according to EN 60950-1.

HARTMANN PXIe 3U 8slot series backplanes are not end-products with independent functionality according the EMC regulations, therefore CE marking is not required. Not before CPCI / PXI Express boards are plugged into the backplane, the systems fulfill the requirements in accordance with EMC Directive 2004/108/EG and Low-voltage Directive 2006/95/EG.

With the EMC optimized enclosure design and the high quality power input filters for the mains connection offers HARTMANN PXI Express backplane serve an ideal base for system Integrators, which comply with the limits of EN 61000-6-3 and EN 61000-6-2

A functionality test is carried out on each system.

# 4. Specification

## *Electrical*

### DC Input through 24 Pin ATX power connector

Main Power: +3.3V, +5V, +12V, -12V
Aux Power: +5V_AUX

### Power available for backplane

The power is limited through the ATX 24 pin power-interface connector.
Refer to the ATX specification for limiting power restrictions.

## System synchronization clocks

**PXI_CLK10**

| | |
|---|---|
| Maximum slot-to-slot skew: | 250 ps |
| Accuracy: | ± 25 ppm |
| Duty-factor: | 45 % - 55 % |

**PXIe_CLK100**

| | |
|---|---|
| Maximum slot-to-slot skew: | 100ps |
| Accuracy: | ± 25 ppm |
| Duty-factor: | 45%-55% |

**PXIe_SYNC100**

| | |
|---|---|
| Maximum slot-to-slot skew: | 100 ps |
| Accuracy: | ± 25 ppm |
| Duty-factor: | 45 %-55 % |

## Electromagnetic compatibility

- EN 61326-1 (IEC 61326-1): Class A emission
- EN 55011 (CISPR 11): Group 1, Class A emission
- EN 55022 (CISPR 22): Class A emission
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emission
- AS/NZS CISPR 22: Class A emission
- FCC 47 CFR Part 15B: Class A Emission
- ICES-001: Class A emission

## *Mechanical*

The backplane has a height of 3U and a width of 36HP according to the 19” sub rack specification.

Figure 6-1 PXIe 3U 8slot series backplane dimensions front (dimensions in millimeter).

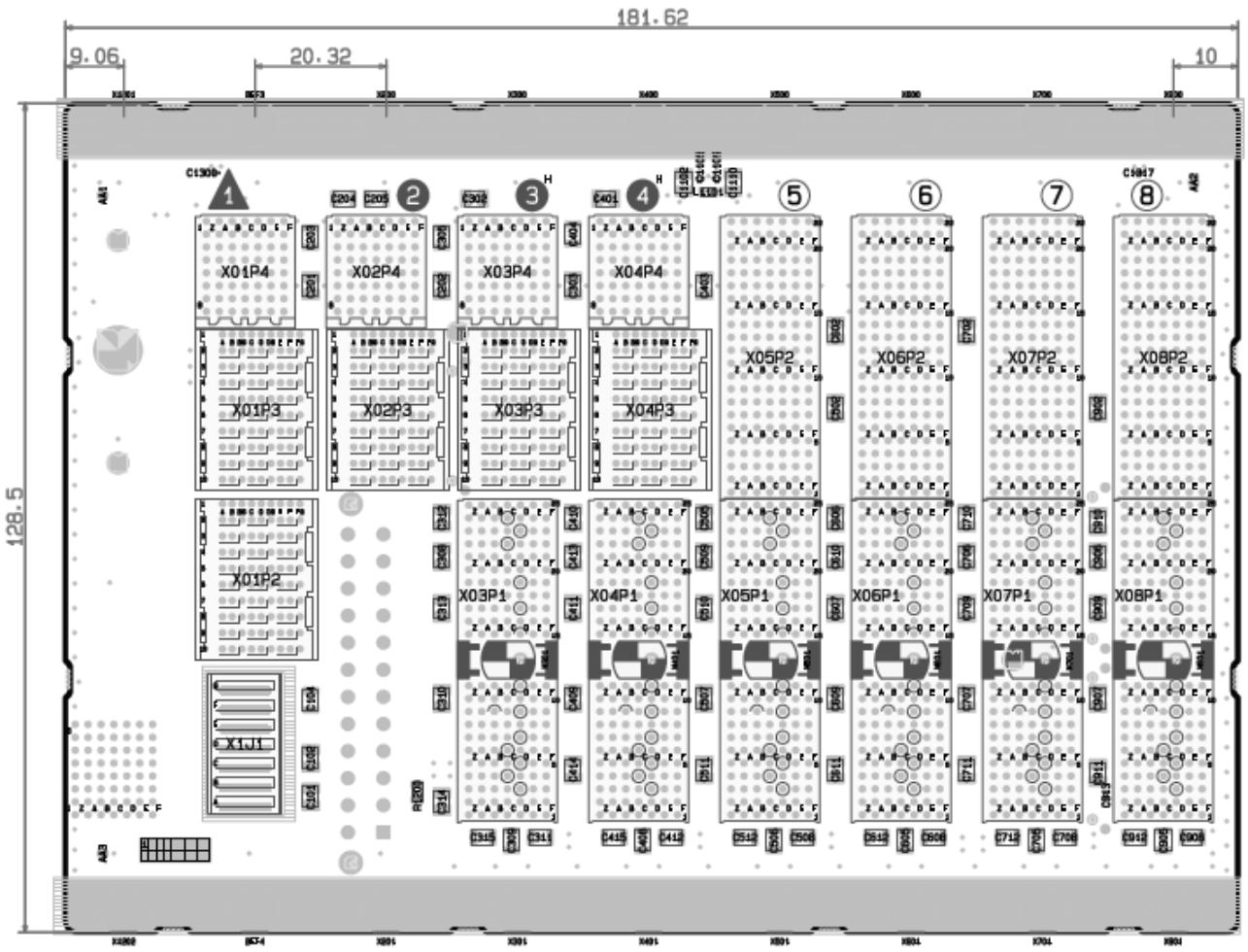
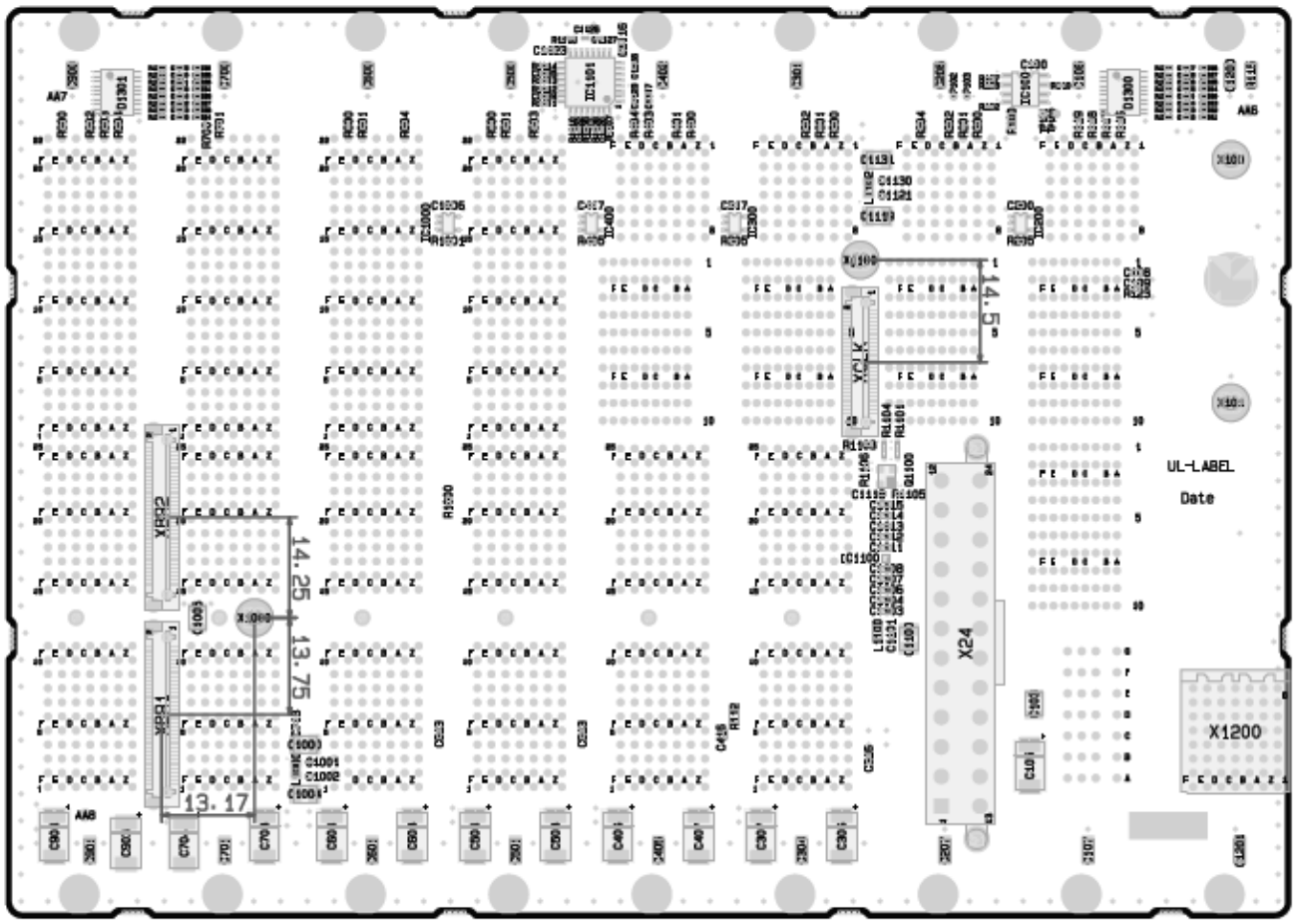


Figure 6-2 PXIe 3U 8slot series backplane dimensions rear side (dimensions in millimeter).




PXIe 3U 8slot series backplane thickness (Dimensions in millimeter).

Backplane thickness: 2.60 mm ±10 %

# *Operating environment*

## Airflow

Airflow from right to left.

**Caution!**

To ensure proper air flow within the system make sure that all slots are populated with either boards or filler panels.

## Humidity

Operating: 5% to 95% non-condensing
Storage: 5% to 95% non-condensing
Tested in accordance with IEC-60068-2-56

## Operational shock

30g peak, half sine, 11ms pulse (Tested in accordance with IEC-60068-2-27.
Meets MIL-PRF-28800F class 2 limits)

## Temperature

Operating temperature range: -40 °C… +85 °C
Storage temperature range: -40 °C… +105 °C

## Random vibration

5 to 500 MHz, 0.3 $g_{RMS}$

## Safety

EN 61010-1, IEC 61010-1, UL 61010-1, CSA 61010-1

# 5. Pin assignment

The Pin assignment applies with the *PXI-5 PXI Express Hardware* specification and the *CompactPCI PICMG 2.0 R. 3.0* specification.

- PXI Express system controller slot (4 Link Configuration)
- PXI Express Hybrid peripheral slot
- PXI Express peripheral slot
- PXI legacy slot
- 24 Pin ATX power connector
- Chassis management connector

## *PXI Express system controller slot (4 Link Configuration)*

| Pin | Z | A | B | C | D | E | F | |
|---|---|---|---|---|---|---|---|---|
| 1 | GND | GA4 | GA3 | GA2 | GA1 | GA0 | GND | **XP4 Connector** |
| 2 | GND | +5Vaux | GND | SYSEN# | WAKE# | ALERT# | GND | |
| 3 | GND | RSV | RSV | RSV | RSV | RSV | GND | |
| 4 | GND | RSV | RSV | RSV | RSV | RSV | GND | |
| 5 | GND | PXI_TRIG3 | PXI_TRIG4 | PXI_TRIG5 | GND | PXI_TRIG6 | GND | |
| 6 | GND | PXI_TRIG2 | GND | RSV | NC | PXI_CLK10 | GND | |
| 7 | GND | PXI_TRIG1 | PXI_TRIG0 | RSV | GND | PXI_TRIG7 | GND | |
| 8 | GND | RSV | GND | RSV | RSV | PXI_LBR6 | GND | |

| Pin | A | B | ab | C | D | cd | E | F | ef | |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | RSV | RSV | GND | RSV | RSV | GND | RSV | RSV | GND | **XP3 Connector** |
| 2 | RSV | RSV | GND | PWR_OK | PS_ON# | GND | LINKCAP | PWRBTN# | GND | |
| 3 | SMBDAT | SMBCLK | GND | 4REFCLK+ | 4REFCLK- | GND | 2REFCLK+ | 2REFCLK- | GND | |
| 4 | RSV | PERST# | GND | 3REFCLK+ | 3REFCLK- | GND | 1REFCLK+ | 1REFCLK- | GND | |
| 5 | 1PETp0 | 1PETn0 | GND | 1PERp0 | 1PERn0 | GND | 1PETp1 | 1PETn1 | GND | |
| 6 | 1PETp2 | 1PETn2 | GND | 1PERp2 | 1PERn2 | GND | 1PERp1 | 1PERn1 | GND | |
| 7 | 1PETp3 | 1PETn3 | GND | 1PERp3 | 1PERn3 | GND | 2PETp0 | 2PETn0 | GND | |
| 8 | 2PETp1 | 2PETn1 | GND | 2PERp1 | 2PERn1 | GND | 2PERp0 | 2PERn0 | GND | |
| 9 | 2PETp2 | 2PETn2 | GND | 2PERp2 | 2PERn2 | GND | 2PETp3 | 2PETn3 | GND | |
| 10 | 3PETp0 | 3PETn0 | GND | 3PERp0 | 3PERn0 | GND | 2PERp3 | 2PERn3 | GND | |

| Pin | A | B | ab | C | D | cd | E | F | ef | |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 3PETp1 | 3PETn1 | GND | 3PERp1 | 3PERn1 | GND | 3PETp2 | 3PETn2 | GND | **XP2 Connector** |
| 2 | 3PETp3 | 3PETn3 | GND | 3PERp3 | 3PERn3 | GND | 3PERp2 | 3PERn2 | GND | |
| 3 | 4PETp0 | 4PETn0 | GND | 4PERp0 | 4PERn0 | GND | NC | NC | GND | |
| 4 | NC | NC | GND | NC | NC | GND | NC | NC | GND | |
| 5 | NC | NC | GND | NC | NC | GND | RSV | RSV | GND | |
| 6 | RSV | RSV | GND | RSV | RSV | GND | RSV | RSV | GND | |
| 7 | RSV | RSV | GND | RSV | RSV | GND | RSV | RSV | GND | |
| 8 | RSV | RSV | GND | RSV | RSV | GND | RSV | RSV | GND | |
| 9 | RSV | RSV | GND | RSV | RSV | GND | RSV | RSV | GND | |
| 10 | RSV | RSV | GND | RSV | RSV | GND | RSV | RSV | GND | |

| Pin | Signals | |
|---|---|---|
| G | GND | **XP1 Connector** |
| F | 12V | |
| E | 12V | |
| D | GND | |
| C | 5V | |
| B | 3.3V | |
| A | GND | |

## *PXI Express hybrid peripheral slot*

| Pin | Z | A | B | C | D | E | F | XP4 Connector |
|---|---|---|---|---|---|---|---|---|
| 1 | GND | GA4 | GA3 | GA2 | GA1 | GA0 | GND | |
| 2 | GND | +5Vaux | GND | SYSEN# | WAKE# | ALERT# | GND | |
| 3 | GND | 12V | 12V | GND | GND | GND | GND | |
| 4 | GND | GND | GND | 3.3V | 3.3V | 3.3V | GND | |
| 5 | GND | PXI_TRIG3 | PXI_TRIG4 | PXI_TRIG5 | GND | PXI_TRIG6 | GND | |
| 6 | GND | PXI_TRIG2 | GND | ATNLED# | NC | PXI_CLK10 | GND | |
| 7 | GND | PXI_TRIG1 | PXI_TRIG0 | ATNSW# | GND | PXI_TRIG7 | GND | |
| 8 | GND | RSV | GND | RSV | PXI_LBL6 | PXI_LBR6 | GND | |

| Pin | A | B | ab | C | D | cd | E | F | ef | XP3 Connector |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | PXIe_CLK100+ | PXIe_CLK100- | GND | PXIe_SYNC100+ | PXIe_SYNC100- | GND | NC | NC | GND | |
| 2 | PRSNT# | PWREN# | GND | NC | NC | GND | NC | NC | GND | |
| 3 | SMBDAT | SMBCLK | GND | RSV | RSV | GND | RSV | RSV | GND | |
| 4 | MPWRGD | PERST# | GND | RSV | RSV | GND | 1REFCLK+ | 1REFCLK- | GND | |
| 5 | 1PETp0 | 1PETn0 | GND | 1PERp0 | 1PERn0 | GND | 1PETp1 | 1PETn1 | GND | |
| 6 | 1PETp2 | 1PETn2 | GND | 1PERp2 | 1PERn2 | GND | 1PERp1 | 1PERn1 | GND | |
| 7 | 1PETp3 | 1PETn3 | GND | 1PERp3 | 1PERn3 | GND | 1PETp4 | 1PETn4 | GND | |
| 8 | 1PETp5 | 1PETn5 | GND | 1PERp5 | 1PERn5 | GND | 1PERp4 | 1PERn4 | GND | |
| 9 | 1PETp6 | 1PETn6 | GND | 1PERp6 | 1PERn6 | GND | 1PETp7 | 1PETn7 | GND | |
| 10 | RSV | RSV | GND | RSV | RSV | GND | 1PERp7 | 1PERn7 | GND | |

| Pin | Z | A | B | C | D | E | F | P1 Connector |
|---|---|---|---|---|---|---|---|---|
| 25 | GND | 5V | REQ64# | ENUM# | 3.3V | 5V | GND | |
| 24 | GND | AD[1] | 5V | V(I/O) | AD[0] | ACK64# | GND | |
| 23 | GND | 3.3V | AD[4] | AD[3] | 5V | AD[2] | GND | |
| 22 | GND | AD[7] | GND | 3.3V | AD[6] | AD[5] | GND | |
| 21 | GND | 3.3V | AD[9] | AD[8] | M66EN | C/BE[0]# | GND | |
| 20 | GND | AD[12] | GND | V(I/O) | AD[11] | AD[10] | GND | |
| 19 | GND | 3.3V | AD[15] | AD[14] | GND | AD[13] | GND | |
| 18 | GND | SERR# | GND | 3.3V | PAR | C/BE[1]# | GND | |
| 17 | GND | 3.3V | IPMB_SCL | IPMB_SDA | GND | PERR# | GND | |
| 16 | GND | DEVSEL# | GND | V(I/O) | STOP# | LOCK# | GND | |
| 15 | GND | 3.3V | FRAME# | IRDY# | BD_SEL# | TRDY# | GND | |
| 12-14 | Key Area | | | | | | | |
| 11 | GND | AD[18] | AD[17] | AD[16] | GND | C/BE[2]# | GND | |
| 10 | GND | AD[21] | GND | 3.3V | AD[20] | AD[19] | GND | |
| 9 | GND | C/BE[3]# | IDSEL | AD[23] | GND | AD[22] | GND | |
| 8 | GND | AD[26] | GND | V(I/O) | AD[25] | AD[24] | GND | |
| 7 | GND | AD[30] | AD[29] | AD[28] | GND | AD[27] | GND | |
| 6 | GND | REQ# | GND | 3.3V | CLK | AD[31] | GND | |
| 5 | GND | BRSVP1A5 | BRSVP1B5 | RST# | GND | GNT# | GND | |
| 4 | GND | IPMB_PWR | HEALTHY# | V(I/O) | INTP | INTS | GND | |
| 3 | GND | INTA# | INTB# | INTC# | 5V | INTD# | GND | |
| 2 | GND | TCK | 5V | TMS | TDO | TDI | GND | |
| 1 | GND | 5V | -12V | TRST# | +12V | 5V | GND | |

## *PXIe peripheral slot*

| Pin | Z | A | B | C | D | E | F | XP4 Connector |
|---|---|---|---|---|---|---|---|---|
| 1 | GND | GA4 | GA3 | GA2 | GA1 | GA0 | GND | |
| 2 | GND | +5Vaux | GND | SYSEN# | WAKE# | ALERT# | GND | |
| 3 | GND | 12V | 12V | GND | GND | GND | GND | |
| 4 | GND | GND | GND | 3.3V | 3.3V | 3.3V | GND | |
| 5 | GND | PXI_TRIG3 | PXI_TRIG4 | PXI_TRIG5 | GND | PXI_TRIG6 | GND | |
| 6 | GND | PXI_TRIG2 | GND | ATNLED# | NC | PXI_CLK10 | GND | |
| 7 | GND | PXI_TRIG1 | PXI_TRIG0 | ATNSW# | GND | PXI_TRIG7 | GND | |
| 8 | GND | RSV | GND | RSV | PXI_LBL6 | PXI_LBR6 | GND | |

| Pin | A | B | ab | C | D | cd | E | F | ef | XP3 Connector |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | PXIe_CLK100+ | PXIe_CLK100- | GND | PXIe_SYNC100+ | PXIe_SYNC100- | GND | NC | NC | GND | |
| 2 | PRSNT# | PWREN# | GND | NC | NC | GND | NC | NC | GND | |
| 3 | SMBDAT | SMBCLK | GND | RSV | RSV | GND | RSV | RSV | GND | |
| 4 | MPWRGD | PERST# | GND | RSV | RSV | GND | 1REFCLK+ | 1REFCLK- | GND | |
| 5 | 1PETp0 | 1PETn0 | GND | 1PERp0 | 1PERn0 | GND | 1PETp1 | 1PETn1 | GND | |
| 6 | 1PETp2 | 1PETn2 | GND | 1PERp2 | 1PERn2 | GND | 1PERp1 | 1PERn1 | GND | |
| 7 | 1PETp3 | 1PETn3 | GND | 1PERp3 | 1PERn3 | GND | 1PETp4 | 1PETn4 | GND | |
| 8 | 1PETp5 | 1PETn5 | GND | 1PERp5 | 1PERn5 | GND | 1PERp4 | 1PERn4 | GND | |
| 9 | 1PETp6 | 1PETn6 | GND | 1PERp6 | 1PERn6 | GND | 1PETp7 | 1PETn7 | GND | |
| 10 | RSV | RSV | GND | RSV | RSV | GND | 1PERp7 | 1PERn7 | GND | |

## *PXI legacy slot*

| Pin | Z | A | B | C | D | E | F | |
|---|---|---|---|---|---|---|---|---|
| 22 | 22 | GND | GA4 | GA3 | GA2 | GA1 | GA0 | P2 Connector |
| 21 | | | | | | | | |
| 20 | 21 | GND | PXI_LBR0 | RSV | PXI_LBR1 | PXI_LBR2 | PXI_LBR3 | |
| 19 | 20 | GND | PXI_LBR4 | PXI_LBR5 | PXI_LBL0 | GND | PXI_LBL1 | |
| 18 | 19 | GND | PXI_LBL2 | RSV | PXI_LBL3 | PXI_LBL4 | PXI_LBL5 | |
| 17 | 18 | GND | PXI_TRIG3 | PXI_TRIG4 | PXI_TRIG5 | GND | PXI_TRIG6 | |
| 16 | 17 | GND | PXI_TRIG2 | GND | RSV | PXI_STAR | PXI_CLK10 | |
| 15 | 16 | GND | PXI_TRIG1 | PXI_TRIG0 | RSV | GND | PXI_TRIG7 | |
| 14 | 15 | GND | PXI_BRSVA15 | GND | RSV | PXI_LBL6 | PXI_LBR6 | |
| 13 | 14 | GND | RSV | RSV | RSV | GND | RSV | |
| 12 | 13 | GND | RSV | GND | V(I/O) | RSV | RSV | |
| 11 | 12 | GND | RSV | RSV | RSV | GND | RSV | |
| 10 | 11 | GND | RSV | GND | V(I/O) | RSV | RSV | |
| 9 | 10 | GND | RSV | RSV | RSV | GND | RSV | |
| 8 | 9 | GND | RSV | GND | V(I/O) | RSV | RSV | |
| 7 | 8 | GND | RSV | RSV | RSV | GND | RSV | |
| 6 | 7 | GND | RSV | GND | V(I/O) | RSV | RSV | |
| 5 | 6 | GND | RSV | RSV | RSV | GND | RSV | |
| 4 | 5 | GND | RSV | 64EN# | V(I/O) | RSV | RSV | |
| 3 | 4 | GND | V(I/O) | PXI_BRSVB4 | RSV | GND | RSV | |
| 2 | 3 | GND | PXI_LBR7 | GND | PXI_LBR8 | PXI_LBR9 | PXI_LBR10 | |
| 1 | 2 | GND | PXI_LBR11 | PXI_LBR12 | UNC | PXI_LBL7 | PXI_LBL8 | |

| Pin | Z | A | B | C | D | E | F | P1 Connector |
|---|---|---|---|---|---|---|---|---|
| 25 | GND | 5V | REQ64# | ENUM# | 3.3V | 5V | GND | |
| 24 | GND | AD[1] | 5V | V(I/O) | AD[0] | ACK64# | GND | |
| 23 | GND | 3.3V | AD[4] | AD[3] | 5V | AD[2] | GND | |
| 22 | GND | AD[7] | GND | 3.3V | AD[6] | AD[5] | GND | |
| 21 | GND | 3.3V | AD[9] | AD[8] | M66EN | C/BE[0]# | GND | |
| 20 | GND | AD[12] | GND | V(I/O) | AD[11] | AD[10] | GND | |
| 19 | GND | 3.3V | AD[15] | AD[14] | GND | AD[13] | GND | |
| 18 | GND | SERR# | GND | 3.3V | PAR | C/BE[1]# | GND | |
| 17 | GND | 3.3V | IPMB_SCL | IPMB_SDA | GND | PERR# | GND | |
| 16 | GND | DEVSEL# | GND | V(I/O) | STOP# | LOCK# | GND | |
| 15 | GND | 3.3V | FRAME# | IRDY# | BD_SEL# | TRDY# | GND | |
| 12-14 | Key Area | | | | | | | |
| 11 | GND | AD[18] | AD[17] | AD[16] | GND | C/BE[2]# | GND | |
| 10 | GND | AD[21] | GND | 3.3V | AD[20] | AD[19] | GND | |
| 9 | GND | C/BE[3]# | IDSEL | AD[23] | GND | AD[22] | GND | |
| 8 | GND | AD[26] | GND | V(I/O) | AD[25] | AD[24] | GND | |
| 7 | GND | AD[30] | AD[29] | AD[28] | GND | AD[27] | GND | |
| 6 | GND | REQ# | GND | 3.3V | CLK | AD[31] | GND | |
| 5 | GND | BRSVP1A5 | BRSVP1B5 | RST# | GND | GNT# | GND | |
| 4 | GND | IPMB_PWR | HEALTHY# | V(I/O) | INTP | INTS | GND | |
| 3 | GND | INTA# | INTB# | INTC# | 5V | INTD# | GND | |
| 2 | GND | TCK | 5V | TMS | TDO | TDI | GND | |
| 1 | GND | 5V | -12V | TRST# | +12V | 5V | GND | |

## *24 pin ATX power connector*

Connector type: Molex, 44206-0007

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +3.3 V | 13 | +3.3 V |
| 2 | +3.3 V | 14 | -12 V |
| 3 | GND | 15 | GND |
| 4 | +5 V | 16 | PS_ON# |
| 5 | GND | 17 | GND |
| 6 | +5 V | 18 | GND |
| 7 | GND | 19 | GND |
| 8 | PWR_OK | 20 | NC |
| 9 | +5V_AUX | 21 | +5 V |
| 10 | +12 V | 22 | +5 V |
| 11 | +12 V | 23 | +5 V |
| 12 | 3.3 V | 24 | GND |

## *Chassis management interface connector*

Connector type: Erni, eHM-M2-HP 214431

| Pin | Z | A | B | C | D | E | F | |
|---|---|---|---|---|---|---|---|---|
| 1 | GND | GND | GND | GND | GND | GND | GND | **XP4 Connector** |
| 2 | GND | +5Vaux | GND | PWR_OK | PWRBTN# | PS_ON# | GND | |
| 3 | GND | +12V | +12V | GND | GND | GND | GND | |
| 4 | GND | GND | GND | +3V3 | +3V3 | +3V3 | GND | |
| 5 | GND | PXI_STAR[4] | PXI_STAR[5] | PXI_STAR[6] | GND | PXI_STAR[7] | GND | |
| 6 | GND | PXI_STAR[3] | GND | IPMB_SCL | PE_PERST# | PXI_CLK10 | GND | |
| 7 | GND | PXI_STAR[2] | PXI_STAR[1] | IPMB_SDA | GND | PXI_STAR[8] | GND | |
| 8 | GND | PXI_CLK10_IN | GND | -12V | GND | GND | GND | |

The corresponding PXI_STAR[x] signal is routed, through a single line and 1:1, to the corresponding slot[x].

Example:
PXI_STAR[3] is routed through a single line to slot 3 on the backplane.

# 6. Ordering information

| Ordering Numbers | Description | PCI V(I/O) |
|---|---|---|
| PXEB38EA10 | PXCe1008 PXIe 8-Slot 3U incl. Bridge-,Clock module | +5V |