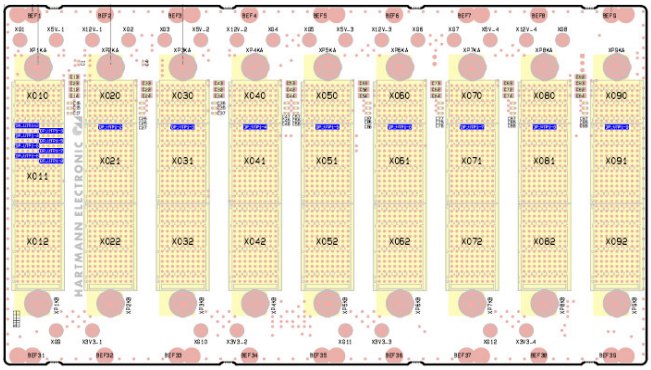
3U OpenVPX BACKPLANE **BKP3-CEN09-15.2.11-3**	**VITA 46** **VITA 65**	

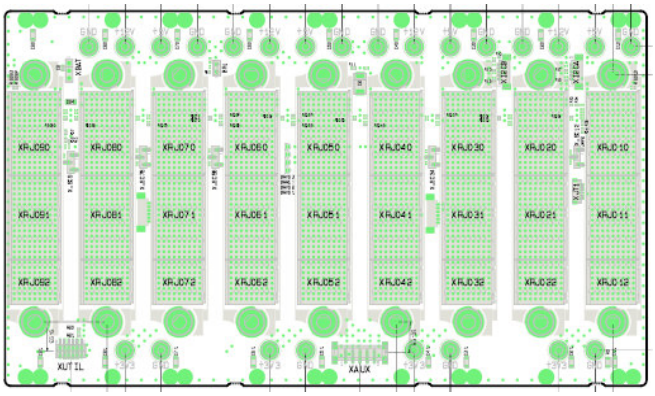
Key Features:

- Compliant to VITA 46.0 baseline specification
- Compliant to VITA 65 OpenVPX, BKP3-CEN09-15.2.11-3
- 9 Slots VPX, 1 Payload Slot, 8 Peripheral Slots
- Configuration Data Plane: Single Star (1x UTP)
- M3 studs for power entry
- PCB size 128.50mm x 225.45mm x 5.4 mm
- 5 HP from slot to slot (25.40 mm)
- Flexible keying and alignment mechanism
- with geographical address pins
- Reference clock
- Auxilary clock
- System Reset
- With JTAG connector on first slot (JT1)
- System Management Interface on the backplane (I2CA, I2CB)
- Non-Volatile Memory Read Only signal set by Jumper BR1
- Battery backup option setting by Jumper XBAT. Vbat external or connected to 3.3 AUX.
- Max. Input current per backplane
  VS1:VS2:VS3 = 120A : 120A : 120A
- Operating temperature: -40° - +85°C
- Storage temperature: -55°C - +85°C
- Flammability rating: UL94-V0
- Custom assembly or modification on request

Front side



Back side



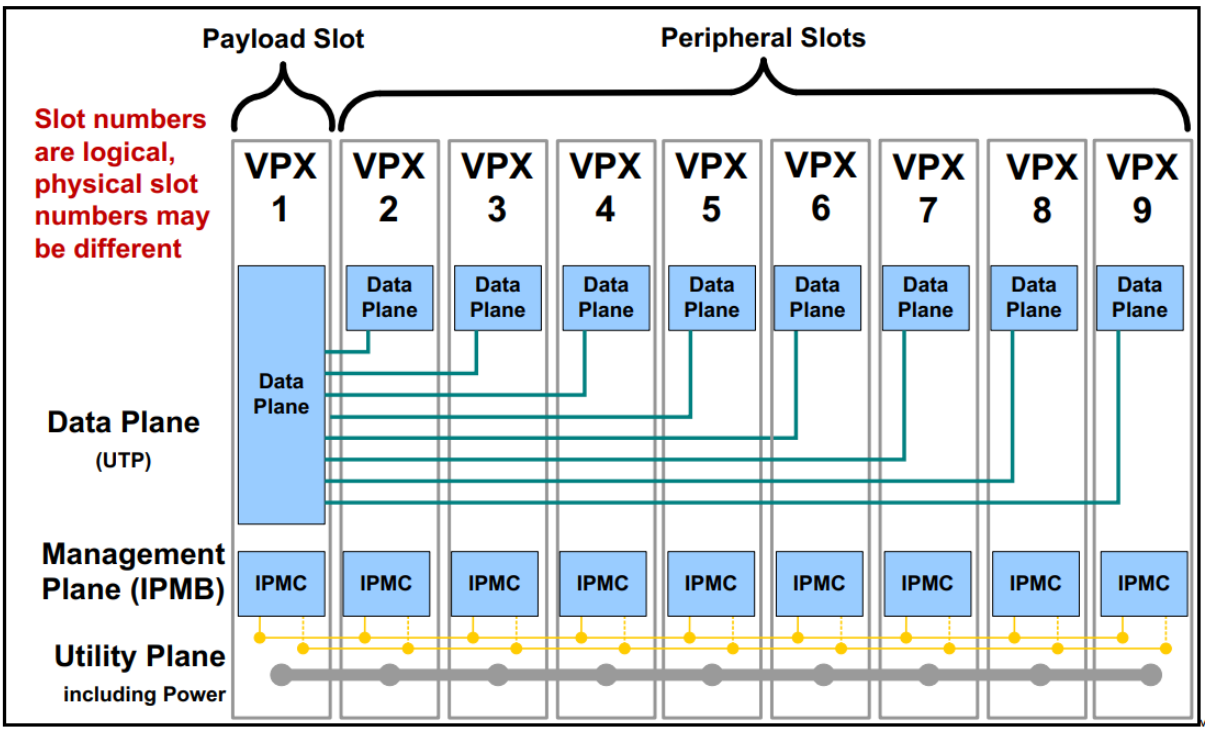
- **Order number: B193901760**

3U OpenVPX BACKPLANE **BKP3-CEN09-15.2.11-3**	**VITA 46** **VITA 65**	

1) Topology: 9-Slot — BKP3-CEN09-15.2.11-3 (1 Payload + 8 Peripheral)

Profile Payload slot: SLT3-PAY-8U-14.2.9 / MOD3-PAY-8U-16.2.9

Profile Peripheral slots: SLT3-PER-1U-14.3.3 / MOD3-PER-1U-16.3.3



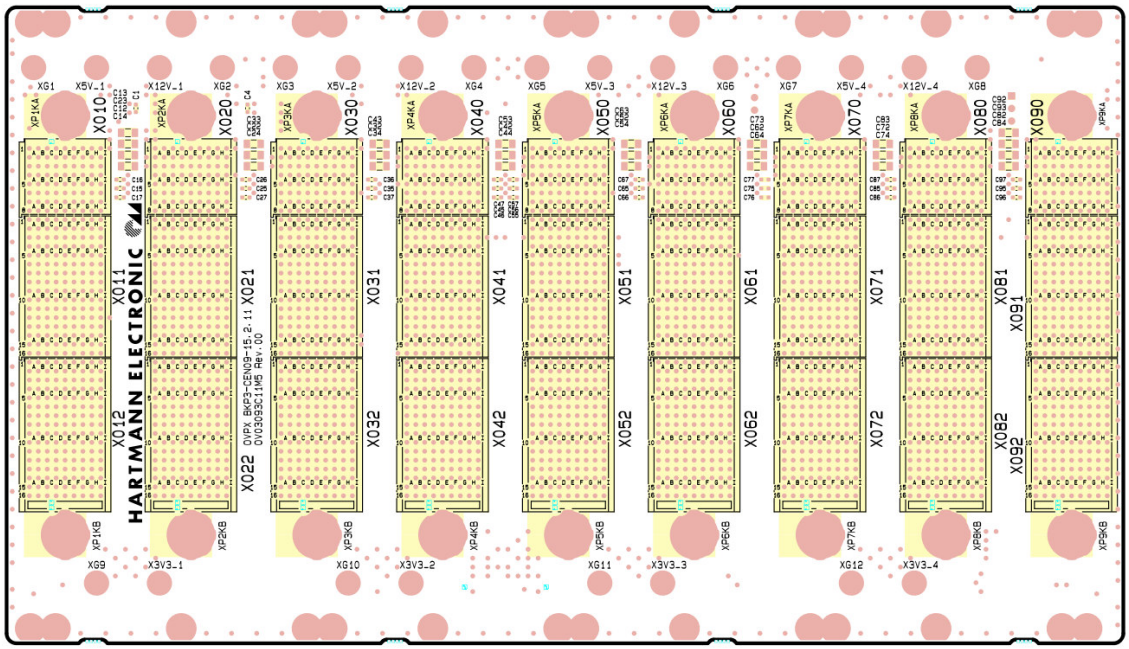
2) Data Plane Port connections

Logical Payload Slot	Peripheral Data Plane Port	Payload Data Plane Port
2	DP01	DP01
3	DP01	DP02
4	DP01	DP03
5	DP01	DP04
6	DP01	DP05
7	DP01	DP06
8	DP01	DP07
9	DP01	DP08

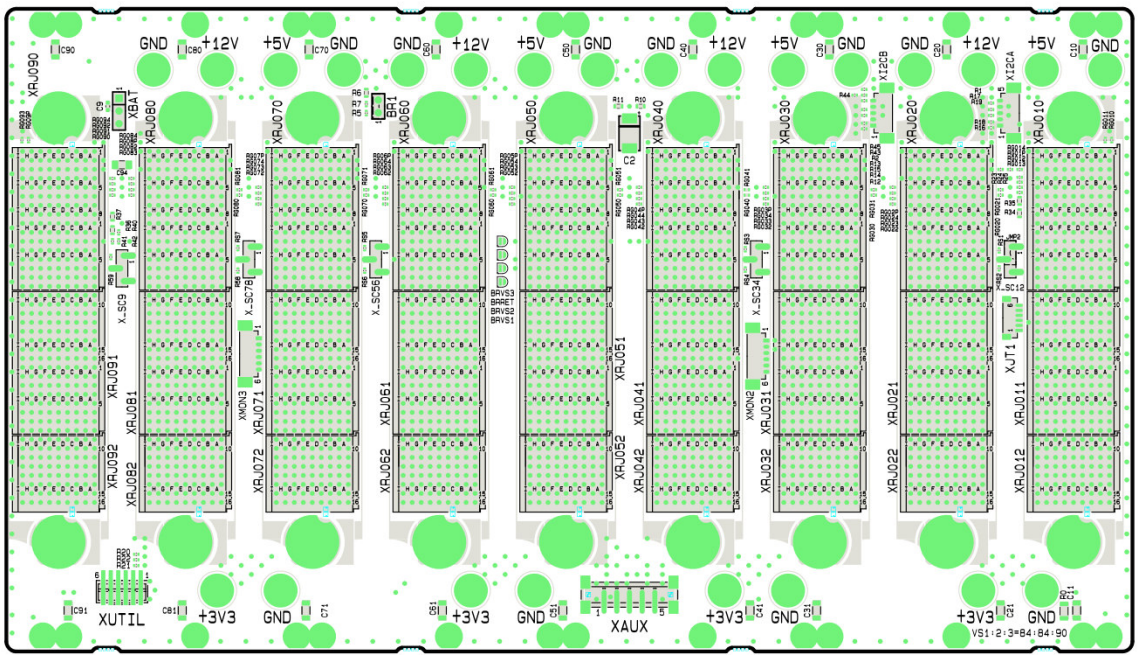
3U OpenVPX BACKPLANE **BKP3-CEN09-15.2.11-3**	**VITA 46** **VITA 65**	

3) Drawings

Front side



Back side



3U OpenVPX BACKPLANE	**VITA 46**	
BKP3-CEN09-15.2.11-3	**VITA 65**	

4) Pin Assignment

Pin Assignment VPX J0 (Utility Connector)

	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Vs1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad*	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

VS1=12V , VS2=3.3V , VS3=5V

Payload Slot Profile SLT3-PAY-8U-14.2.9— P1 & J1

Plug-In Module P1		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1 – 4	GDiscrete1	GND	*GND-J1*	DP01-T+	DP01-T+	GND	*GND-J1*	DP01-T+	DP01-T+
2		GND	DP02-T+	DP02-T+	*GND-J1*	GND	DP02-T+	DP02-T+	*GND-J1*	GND
3		P1-VBAT	GND	*GND-J1*	DP03-T+	DP03-T+	GND	*GND-J1*	DP03-T+	DP03-T+
4		GND	DP04-T+	DP04-T+	*GND-J1*	GND	DP04-T+	DP04-T+	*GND-J1*	GND
5	Data Plane Port 5 – 8	SYS_CON*	GND	*GND-J1*	DP05-T+	DP05-T+	GND	*GND-J1*	DP05-T+	DP05-T+
6		GND	DP06-T+	DP06-T+	*GND-J1*	GND	DP06-T+	DP06-T+	*GND-J1*	GND
7		Reserved	GND	*GND-J1*	DP07-T+	DP07-T+	GND	*GND-J1*	DP07-T+	DP07-T+
8		GND	DP08-T+	DP08-T+	*GND-J1*	GND	DP08-T+	DP08-T+	*GND-J1*	GND
9	User Defined	UD	GND	*GND-J1*	UD	UD	GND	*GND-J1*	UD	UD
10		GND	UD	UD	*GND-J1*	GND	UD	UD	*GND-J1*	GND
11		UD	GND	*GND-J1*	UD	UD	GND	*GND-J1*	UD	UD
12		GND	UD	UD	*GND-J1*	GND	UD	UD	*GND-J1*	GND
13		UD	GND	*GND-J1*	UD	UD	GND	*GND-J1*	UD	UD
14		GND	UD	UD	*GND-J1*	GND	UD	UD	*GND-J1*	GND
15		Maskable Reset*	GND	*GND-J1*	UD	UD	GND	*GND-J1*	UD	UD
16		GND	UD	UD	*GND-J1*	GND	UD	UD	*GND-J1*	GND

Payload Slot Profile SLT3-PAY-8U-14.2.9— P2 & J2

This connector is all User Defined pins. See Section 6.3.3 for requirements and pin assignments Concerning connectors that are all User Defined.
Connector Example Combined Plug-In Module & Backplane - Differential

Backplane Jn	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	UD	UD	UD	UD	UD	GND	UD	UD	UD
2	GND	UD	UD	GND	UD	UD	UD	UD	GND
3	UD	UD	UD	UD	UD	GND	UD	UD	UD
4	GND	UD	UD	GND	UD	UD	UD	UD	GND
5	UD	UD	UD	UD	UD	GND	UD	UD	UD
6	GND	UD	UD	GND	UD	UD	UD	UD	GND
7	UD	UD	UD	UD	UD	GND	UD	UD	UD
8	GND	UD	UD	GND	UD	UD	UD	UD	GND
9	UD	UD	UD	UD	UD	GND	UD	UD	UD
10	GND	UD	UD	GND	UD	UD	UD	UD	GND
11	UD	UD	UD	UD	UD	GND	UD	UD	UD
12	GND	UD	UD	GND	UD	UD	UD	UD	GND
13	UD	UD	UD	UD	UD	GND	UD	UD	UD
14	GND	UD	UD	GND	UD	UD	UD	UD	GND
15	UD	UD	UD	UD	UD	GND	UD	UD	UD
16	GND	UD	UD	GND	UD	UD	UD	UD	GND

Peripheral Slot Profile SLT3-PER-1U-14.3.3— P1 & J1

Plug-In Module P1		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2	User Defined	GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DU	DU	GND	GND-J1	UD	UD
4		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
5		SYS_CON*	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
6		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
7		Reserved	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
8		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
9		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
16		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND

Peripheral Slot Profile SLT3-PER-1U-14.3.3— P2 & J2

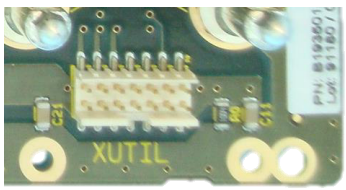
This connector is all User Defined pins. See Section 6.3.3 for requirements and pin assignments Concerning connectors that are all User Defined.
Connector Example Combined Plug-In Module & Backplane - Differential

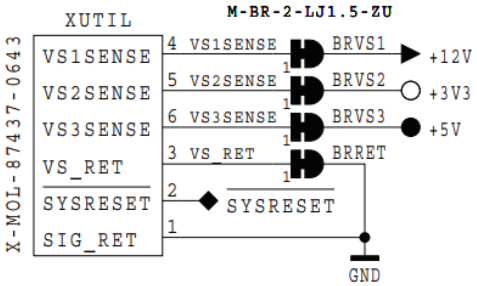
Backplane Jn	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	UD	UD	UD	UD	UD	GND	UD	UD	UD
2	GND	UD	UD	GND	UD	UD	UD	UD	GND
3	UD	UD	UD	UD	UD	GND	UD	UD	UD
4	GND	UD	UD	GND	UD	UD	UD	UD	GND
5	UD	UD	UD	UD	UD	GND	UD	UD	UD
6	GND	UD	UD	GND	UD	UD	UD	UD	GND
7	UD	UD	UD	UD	UD	GND	UD	UD	UD
8	GND	UD	UD	GND	UD	UD	UD	UD	GND
9	UD	UD	UD	UD	UD	GND	UD	UD	UD
10	GND	UD	UD	GND	UD	UD	UD	UD	GND
11	UD	UD	UD	UD	UD	GND	UD	UD	UD
12	GND	UD	UD	GND	UD	UD	UD	UD	GND
13	UD	UD	UD	UD	UD	GND	UD	UD	UD
14	GND	UD	UD	GND	UD	UD	UD	UD	GND
15	UD	UD	UD	UD	UD	GND	UD	UD	UD
16	GND	UD	UD	GND	UD	UD	UD	UD	GND

5) Current Capability:

- +12V 120 A
- +3.3V 120 A
- +5V 120 A
- -12V AUX 9 A
- +12V AUX 9 A
- +3.3V AUX 9 A

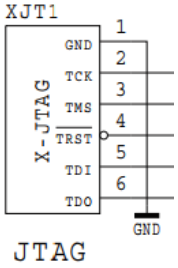
6) UTILITY (Connector XUTIL)





7) JTAG (Connector XJT1)

Consider: JTAG only at Slot 1



8) SYSCON

By setting the signal Syscon to GND the system slot is defined. In general the system slot is slot 1.

There are additional connectors X_SC34, X_SC56 X_SC78 and X_SC9 so as you can select any slot as system slot.

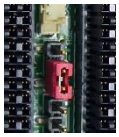
We offer 2 options for setting:

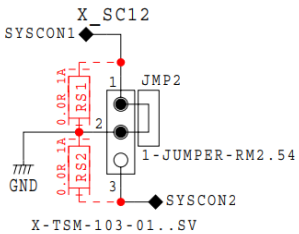
- Jumper (standard)

- 0 Ohm Resistor for rugged applications

X_SC12

1	SYSCON1
2	GND
3	SYSCON2





9) I2C Connector

There are 2 connectors for system-management I2CA and I2CB.

For customer specific board assembly Zero-Ohm resistors available.

Usable voltages for I2C are 3.3V-AUX

I2CA

1	I2CA_SCL
2	GND
3	I2CA_SDA
4	I2CA_PWR
5	NC

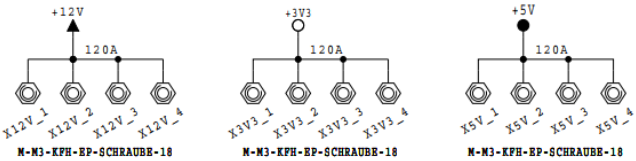
I2CB

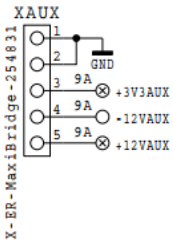
1	I2CB_SCL
2	GND
3	I2CB_SDA
4	I2CB_PWR
5	NC

10) Power Studs M3 / AUX

The main operating voltages (+12V, 3.3V,+5V) and GND are supplied with M3 screw terminals.

The auxiliary operating voltages are supplied via single row vertical terminals. Optimal daughter board supply and trouble-free operation are ensured by the arrangement of the feed modules on the backplane.



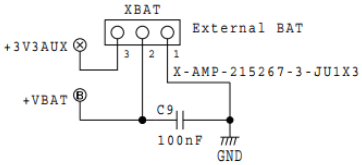


11) XBAT

Normally a battery voltage with approximately 3V is available at Pin VBAT of connector VPX-J1. The voltage is externally accessible with connector XBAT, Pin2 **or** internally using 3.3V_AUX by setting a Jumper between Pin2 and Pin3.

XBAT

1	GND
2	+VBAT
3	+3.3V_AUX

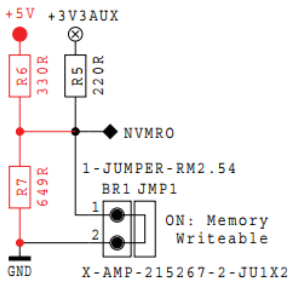


12) NVMRO

If Jumper BR1 is closed NVRMO is set to memory writeable.

BR1

1	NVMRO
2	GND



Germany
Hartmann Electronic GmbH
Phone: +49 711 13 98 90
Fax: +49 711 8 66 11 91
vertrieb.he@kontron.com
www.hartmann-electronic.com

USA
Kontron
Fabian Hemmann
Phone: +1 937-324-2420
Mobile: +1 937 346 7878
fabian.hemmann@us.kontron.com
www.hartmann-electronic.com

France
Kontron Modular Computers S.A.S.
Serge Pichat
Phone: +33 (0)9 66 44 03 15
Mobile: +33 (0)6 82 62 16 00
Serge.pichat@kontron.com
www.hartmann-electronic.com

India
Hartmann Electronic GmbH
Vivek Deshpande
Phone: +1 91 20 66 74 51 23
Vivek.Deshpande@kontron.com
www.hartmann-electronic.com

All data is for information purposes only and not guaranteed for legal purposes. Information has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. Specifications are subject to change without notice.