

3U Open VPX BACKPLANE BKP3-DIS06-15.2.14-3

VITA 46
VITA 65



Key Features:

- Compliant to VITA 46.0 baseline specification
- Compliant to VITA 65 OpenVPX, BKP3-DIS06-15.2.14-n
- 6 Slots VPX, 5 Payload Slots , 1 Switch Slot 
- Configuration Data plane: Data ring for 5 slots (FP)
- Configuration Control plane: Single Star (2x TP/Slot)
- M3 studs for power entry
- PCB size 128.5mm x 153.2mm x 5.4 mm
- 5 HP from slot to slot (25.40 mm)
- Flexible keying and alignment mechanism
- with geographical address pins
- System Management Interface on the backplane (I2CA, I2CB)
- with JTAG connector on first slot
- Reference clock
- Auxiliary clock
- Non-Volatile Memory Read Only signal set by Jumper BR1
- Battery backup option setting by Jumper XBAT. Vbat external or connected to 3.3 AUX.
- Max. Input current per backplane
VS1:VS2:VS3 = 120A : 120 : 120A
(14A/ Slot and Voltage)
- System Reset
- Operating temperature: -40° - +85°C
- Storage temperature: -55°C - +85°C
- Flammability rating: UL94-V0
- Custom assembly or modification on request

Front side



Rear side



▪ **Order number: B193511461**

3U Open VPX
BACKPLANE
BKP3-DIS06-15.2.14-3

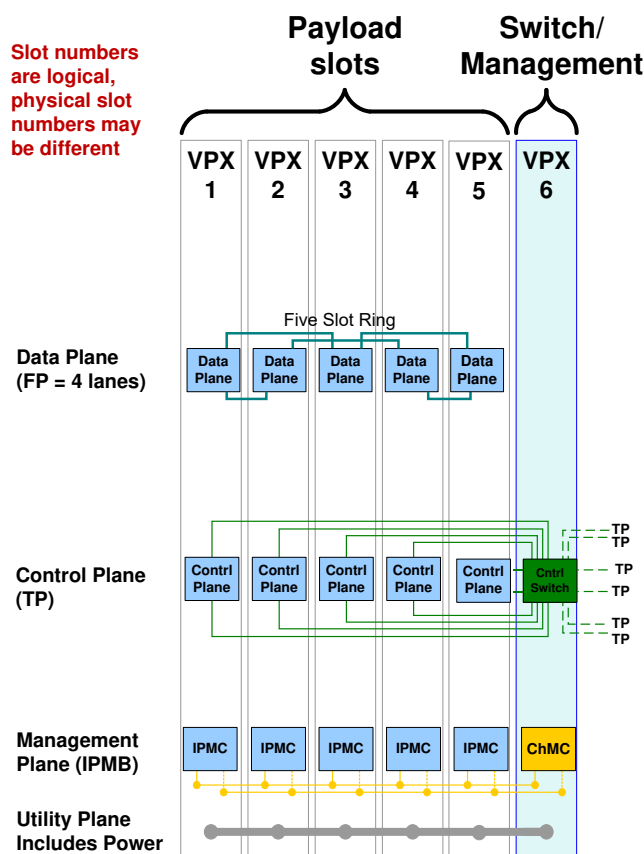
VITA 46
VITA 65



1) Topology: 6-Slot — BKP3-DIS06-15.2.14-n (5 Payload + 1 Switch)

Profile Switch slot: SLT3-SWH-16T-14.4.6 / MOD3-SWH-16T-16.4.7-n

Profile Payload slot: SLT3-PAY-2F2T-14.2.5 / MOD3-PAY-2F2T-16.2.5-n



2) Data Plane Connection BKP3-DIS06-15.2.14-n

Slot/ Channel		DP01	DP02
1	5-Slot Mesh Cluster 1	VPX03-DP01	VPX02-DP02
2		VPX04-DP01	VPX01-DP02
3		VPX01-DP01	VPX05-DP01
4		VPX02-DP01	VPX05-DP02
5		VPX03-DP02	VPX04-DP02

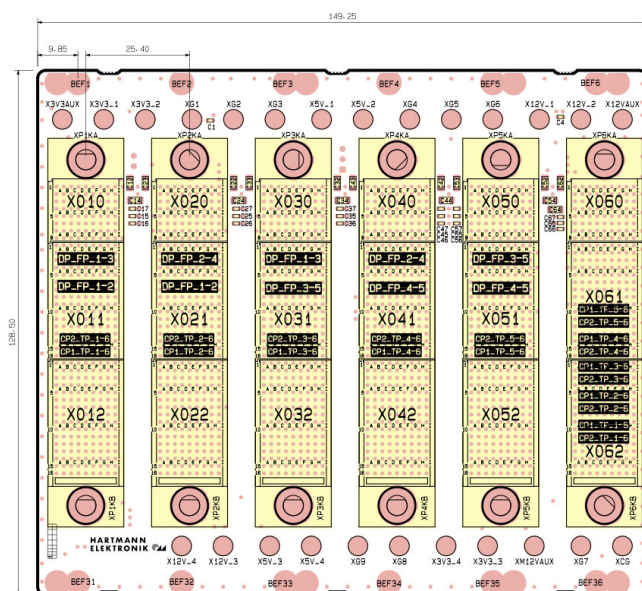
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VITA 46
VITA 65

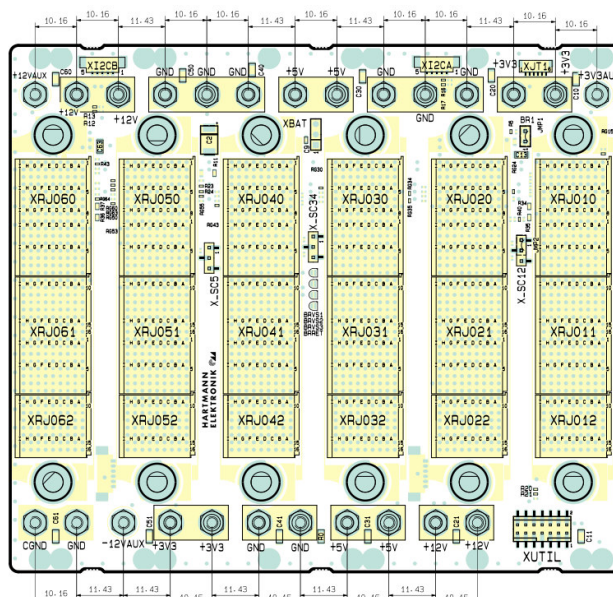


3) Drawings

Front side



Rear side



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BACKPLANE
BKP3-DIS06-15.2.14-3

VITA 46
VITA 65



4) Pin Assignment

Payload Slot Profile SLT3-PAY-2F2T 14.2.5 — P1 & J1

Plug-In Module P1				Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J1				Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	X8	x4 / 2x2 / 4x1	GDiscrete1	GND	GND-J1	DP01-TD1-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2				GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3				P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4				GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Data Plane Port 2	X8	x4 / 2x2 / 4x1	SYS_CON*	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
6				GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
7				Reserved	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
8				GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
9	User Defined			UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10				GND	UD	GND-J1	GND-J1	GND	UD	GND-J1	GND-J1	GND
11				UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12				GND	UD	UD	GND-J1	GND	UD	GND-J1	GND-J1	GND
13	Control Plane			UD	GND	GND-J4	CPtp02-DB-	CPtp02-DB+	GND	GND-J4	CPtp02-DA-	CPtp02-DA+
14				GND	CPtp02-DD-	CPtp02-DD+	GND-J4	GND	CPtp02-DC-	CPtp02-DC+	GND-J4	GND
15				Maskable Reset*	GND	GND-J4	CPtp01-DB-	CPtp01-DB+	GND	GND-J4	CPtp01-DA-	CPtp01-DA+
16				GND	CPtp01-DD-	CPtp01-DD+	GND-J4	GND	CPtp01-DC-	CPtp01-DC+	GND-J4	GND

Universal Ground Pattern User Defined pins for J2 acc. Table 6.3.3.1-5

Backplane J2	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	UD	UD	UD	UD	UD	GND	UD	UD	UD
2	GND	UD	UD	GND	UD	UD	UD	UD	GND
3	UD	UD	UD	UD	UD	GND	UD	UD	UD
4	GND	UD	UD	GND	UD	UD	UD	UD	GND
5	UD	UD	UD	UD	UD	GND	UD	UD	UD
6	GND	UD	UD	GND	UD	UD	UD	UD	GND
7	UD	UD	UD	UD	UD	GND	UD	UD	UD
8	GND	UD	UD	GND	UD	UD	UD	UD	GND
9	UD	UD	UD	UD	UD	GND	UD	UD	UD
10	GND	UD	UD	GND	UD	UD	UD	UD	GND
11	UD	UD	UD	UD	UD	GND	UD	UD	UD
12	GND	UD	UD	GND	UD	UD	UD	UD	GND
13	UD	UD	UD	UD	UD	GND	UD	UD	UD
14	GND	UD	UD	GND	UD	UD	UD	UD	GND
15	UD	UD	UD	UD	UD	GND	UD	UD	UD
16	GND	UD	UD	GND	UD	UD	UD	UD	GND

3U Open VPX BACKPLANE

BKP3-DIS06-15.2.14-3

**VITA 46
VITA 65**



Switch Slot Profile SLT3-SWH-16T-14.4.6— P1& J1

Plug-In Module P1	Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J1	Row i	Row h	Even	Odd	Row e	Row d	Even	Odd	Row a
1	GDiscrete1	GND	GND-J1	TP01-DB-	TP01-DB+	GND	GND-J1	TP01-DA-	TP01-DA+
2	GND	TP01-DD-	TP01-DD+	GND-J1	GND	TP01-DC-	TP01-DC+	GND-J1	GND
3	P1-VBAT	GND	GND-J1	TP02-DB-	TP02-DB+	GND	GND-J1	TP02-DA-	TP02-DA+
4	GND	TP02-DD-	TP02-DD+	GND-J1	GND	TP02-DC-	TP02-DC+	GND-J1	GND
5	SYS_CON*	GND	GND-J1	TP03-DB-	TP03-DB+	GND	GND-J1	TP03-DA-	TP03-DA+
6	GND	TP03-DD-	TP03-DD+	GND-J1	GND	TP03-DC-	TP03-DC+	GND-J1	GND
7	Reserved	GND	GND-J1	TP04-DB-	TP04-DB+	GND	GND-J1	TP04-DA-	TP04-DA+
8	GND	TP04-DD-	TP04-DD+	GND-J1	GND	TP04-DC-	TP04-DC+	GND-J1	GND
9	UD	GND	GND-J1	TP05-DB-	TP05-DB+	GND	GND-J1	TP05-DA-	TP05-DA+
10	GND	TP05-DD-	TP05-DD+	GND-J1	GND	TP05-DC-	TP05-DC+	GND-J1	GND
11	UD	GND	GND-J1	TP06-DB-	TP06-DB+	GND	GND-J1	TP06-DA-	TP06-DA+
12	GND	TP06-DD-	TP06-DD+	GND-J1	GND	TP06-DC-	TP06-DC+	GND-J1	GND
13	UD	GND	GND-J1	TP07-DB-	TP07-DB+	GND	GND-J1	TP07-DA-	TP07-DA+
14	GND	TP07-DD-	TP07-DD+	GND-J1	GND	TP07-DC-	TP07-DC+	GND-J1	GND
15	Maskable Reset*	GND	GND-J1	TP08-DB-	TP08-DB+	GND	GND-J1	TP08-DA-	TP08-DA+
16	GND	TP08-DD-	TP08-DD+	GND-J1	GND	TP08-DC-	TP08-DC+	GND-J1	GND

Switch Slot Profile SLT3-SWH-16T-14.4.6— P2 & J2

Plug-In Module P2	Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J2	Row i	Row h	Even	Odd	Row e	Row d	Even	Odd	Row a
1	UD	GND	GND-J2	TP09-DB-	TP09-DB+	GND	GND-J2	TP09-DA-	TP09-DA+
2	GND	TP09-DD-	TP09-DD+	GND-J2	GND	TP09-DC-	TP09-DC+	GND-J2	GND
3	UD	GND	GND-J2	TP10-DB-	TP10-DB+	GND	GND-J2	TP10-DA-	TP10-DA+
4	GND	TP10-DD-	TP10-DD+	GND-J2	GND	TP10-DC-	TP10-DC+	GND-J2	GND
5	UD	GND	GND-J2	TP11-DB-	TP11-DB+	GND	GND-J2	TP11-DA-	TP11-DA+
6	GND	TP11-DD-	TP11-DD+	GND-J2	GND	TP11-DC-	TP11-DC+	GND-J2	GND
7	UD	GND	GND-J2	TP12-DB-	TP12-DB+	GND	GND-J2	TP12-DA-	TP12-DA+
8	GND	TP12-DD-	TP12-DD+	GND-J2	GND	TP12-DC-	TP12-DC+	GND-J2	GND
9	UD	GND	GND-J2	TP13-DB-	TP13-DB+	GND	GND-J2	TP13-DA-	TP13-DA+
10	GND	TP13-DD-	TP13-DD+	GND-J2	GND	TP13-DC-	TP13-DC+	GND-J2	GND
11	UD	GND	GND-J2	TP14-DB-	TP14-DB+	GND	GND-J2	TP14-DA-	TP14-DA+
12	GND	TP14-DD-	TP14-DD+	GND-J2	GND	TP14-DC-	TP14-DC+	GND-J2	GND
13	UD	GND	GND-J2	TP15-DB-	TP15-DB+	GND	GND-J2	TP15-DA-	TP15-DA+
14	GND	TP15-DD-	TP15-DD+	GND-J2	GND	TP15-DC-	TP15-DC+	GND-J2	GND
15	UD	GND	GND-J2	TP16-DB-	TP16-DB+	GND	GND-J2	TP16-DA-	TP16-DA+
16	GND	TP16-DD-	TP16-DD+	GND-J2	GND	TP16-DC-	TP16-DC+	GND-J2	GND

3U Open VPX BACKPLANE BKP3-DIS06-15.2.14-3	VITA 46 VITA 65	
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Pin Assignment VPX J0 (Utility Connector)

PIN NUMBER	ROW I VPX	ROW H VPX	ROW G VPX	ROW F VPX	ROW E VPX	ROW D VPX	ROW C VPX	ROW B VPX	ROW A VPX
1	VS1	VS1	VS1	VS1	None	VS2	VS2	VS2	VS2
2	VS1	VS1	VS1	VS1	None	VS2	VS2	VS2	VS2
3	VS3	VS3	VS3	VS3	None	VS3	VS3	VS3	VS3
4	GND	SM2	SM3	GND	-12V_AUX	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_AUX	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_AUX	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

VS1=12V , VS2=3.3V , VS3=5V

5) Current Capability:

- +12V

+3.3V

+5V

-12V AUX

+12V AUX

+3.3V AUX

120 A

120 A

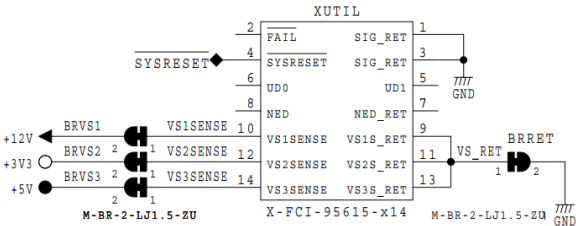
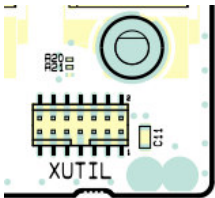
120 A

8 A

8 A

8 A

6) UTILITY (Connector XUTIL)



Connector Amphenol/FCI 95615-014TRLF

7) JTAG (connector XJT1)

For test and programming a JTAG connector (6-poles) is implemented (XJT1).

Connector JST BM06B-SRSS-TB(LF)(SN)

XJT1	Signal
1	GND
2	TCK
3	TMS
4	TRST-
5	TDI
6	TDO



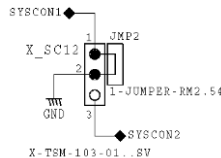
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VITA 46
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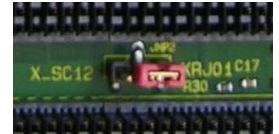
8) SYSCON

By setting the signal Syscon to GND the system slot is defined. In general the system slot is slot1.



JMP2

1	SYSCON1
2	GND
3	SYSCON2



9) I2C connector

There are 2 connectors for system-management I2CA and I2CB.

For customer specific board assembly Zero-Ohm resistors available.

Usable voltages for I2C are 3.3V-AUX

I2CA

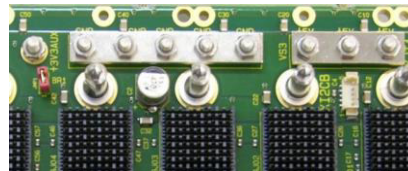
1	I2CA_SCL
2	GND
3	I2CA_SDA
4	I2CA_PWR
5	NC

I2CB

1	I2CB_SCL
2	GND
3	I2CB_SDA
4	I2CB_PWR
5	NC

10) Power Studs M3

The main operating voltages (+12V, +3.3V, +5V) and GND are supplied with M3 screw terminals. The auxiliary operating voltages are supplied via M3 screw terminals.

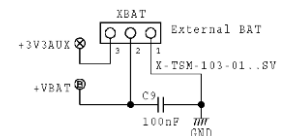


11) XBAT

Normally a battery voltage with approximately 3V is available at Pin VBAT of connector VPX-J1. The voltage is externally accessible with connector XBAT, Pin2 or internally using 3.3V_AUX by setting a Jumper between Pin2 and Pin3.

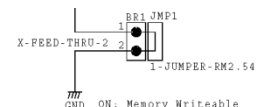
VBAT X5

1	GND
2	+VBAT
3	+3.3V_AUX



BR1

1	NVMRO
2	GND



12) NVMRO

If Jumper BR1 is closed NVRMO is set to memory writeable.

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