

3U Open VPX BACKPLANE BKP3-CEN08-15.2.15-4

VITA 46
VITA 65

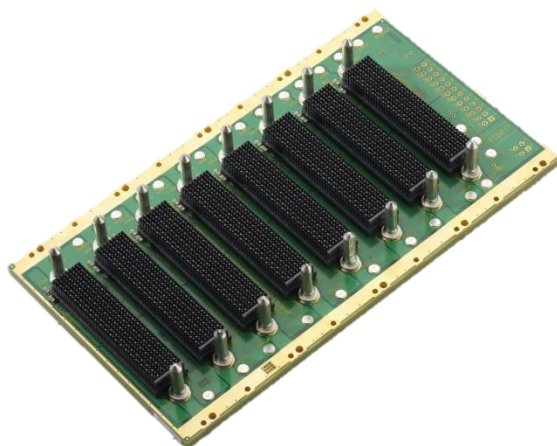


Key figures:

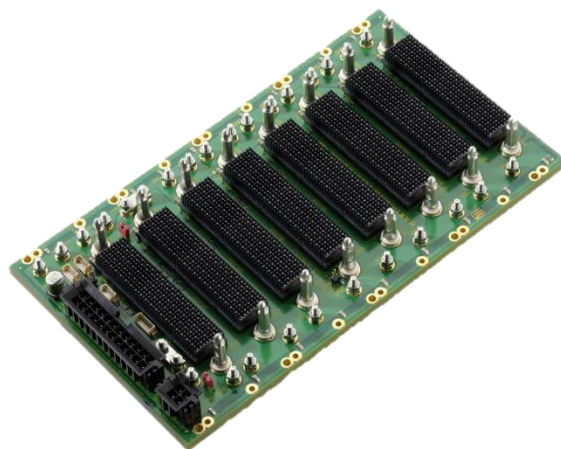
- Compliant to VITA 46.0 baseline specification
- Compliant to VITA 65 Open VPX 2.08 Draft
- 8 Slots VPX, 6 Payload Slots , 2 Switch Slots
- Dual Star X4 configuration
- M3 studs and ATX connector for powerentry
- PCB size 128.5mm x 229.4mm x 5.4 mm
- 5 HP from slot to slot (25.40 mm)
- Flexible keying and alignment mechanism
- System Management Interface on the backplane (I2C1, I2C2)
- with geographical address pins
- Reference clock
- Non-Volatile Memory Read Only signal set by Jumper BR1
- Battery backup option setting by Jumper X5. Vbat external or connected to 3.3 AUX.
- Power Consumption:
VS1:VS2:VS3 = 112A : 112A : 120A
(15A/ Slot and Voltage)
- System Reset
- Operating temperature: -40° - +85°C
- Storage temperature: -55°C - +85°C
- Flammability rating: UL94-V0
- Optional with: +5V termination
- Other configurations on request
- **Order number: B190308011**



Front side



Rear side



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BACKPLANE
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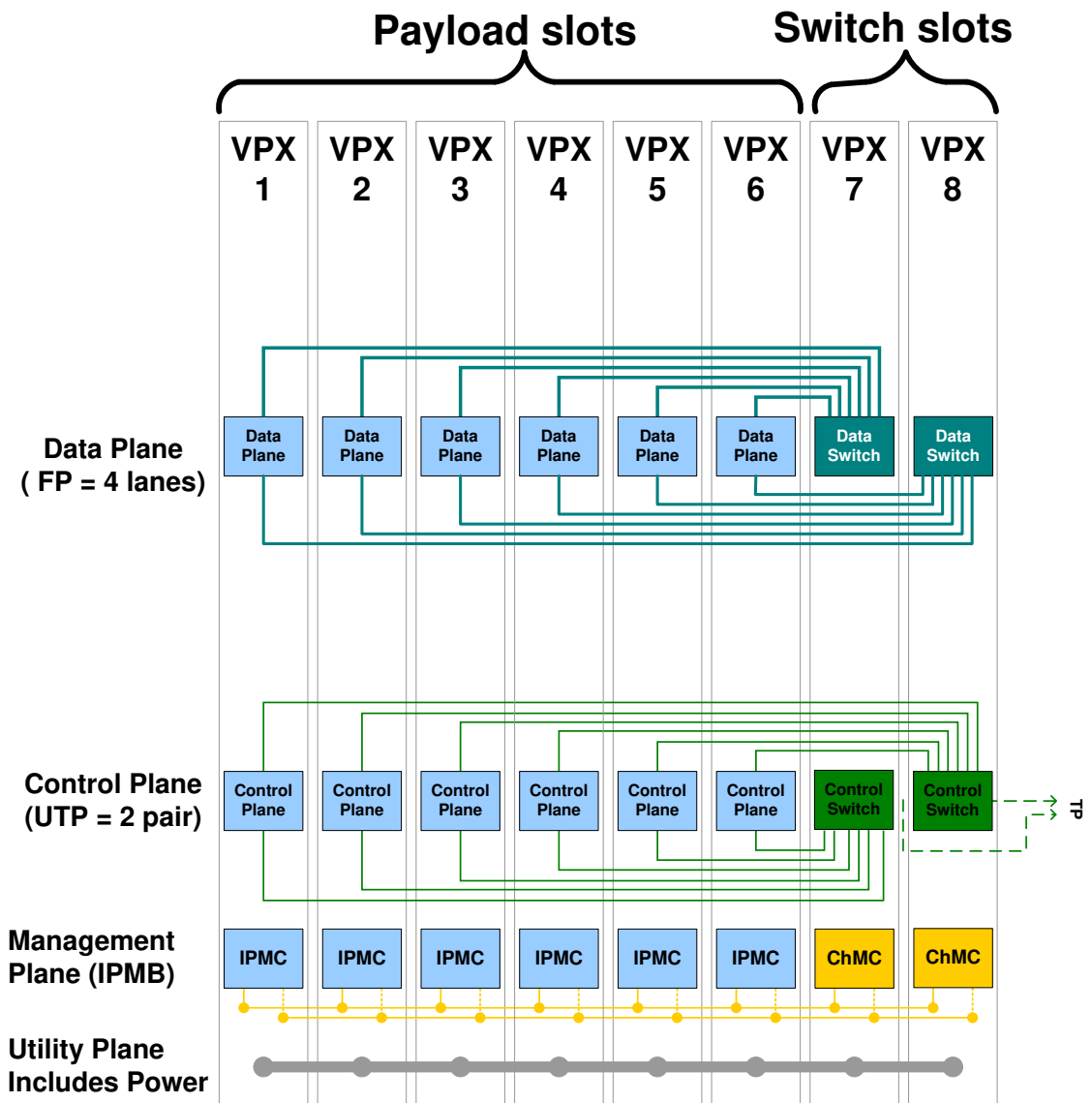
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1) Topology: Dual Star BKP3-CEN08-15.2.15-n
(6 Payloads + 2 integrated Switches)

Profil Switch slots: SLT3-SWH-6F6U-14.4.1

Profil Payload slots: SLT3-PAY-2F2U-14.2.3



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Control Plane Port connections BKP3-CEN08-15.2.15-n

Logical Payload slot	Payload Control Plane Port	Slot 7 Switch Control Plane Port	Slot 8 Switch Control Plane Port
<u>1</u>	CPutp01	CPutp01	
	CPutp02		CPutp01
<u>2</u>	CPutp01	CPutp02	
	CPutp02		CPutp02
<u>3</u>	CPutp01	CPutp03	
	CPutp02		CPutp03
<u>4</u>	CPutp01	CPutp04	
	CPutp02		CPutp04
<u>5</u>	CPutp01	CPutp05	
	CPutp02		CPutp05
<u>6</u>	CPutp01	CSutp01	
	CPutp02		CSutp01

Data Plane Port connections BKP3-CEN08-15.2.15-n

Logical Payload slot	Payload Data Plane Port	Slot 7 Switch Data Plane Port	Slot 8 Switch Data Plane Port
<u>1</u>	<u>DP01</u>	<u>DP01</u>	
	<u>DP02</u>		<u>DP01</u>
<u>2</u>	<u>DP01</u>	<u>DP02</u>	
	<u>DP02</u>		<u>DP02</u>
<u>3</u>	<u>DP01</u>	<u>DP03</u>	
	<u>DP02</u>		<u>DP03</u>
<u>4</u>	<u>DP01</u>	<u>DP04</u>	
	<u>DP02</u>		<u>DP04</u>
<u>5</u>	<u>DP01</u>	<u>DP05</u>	
	<u>DP02</u>		<u>DP05</u>
<u>6</u>	<u>DP01</u>	<u>DS01</u>	
	<u>DP02</u>		<u>DS01</u>

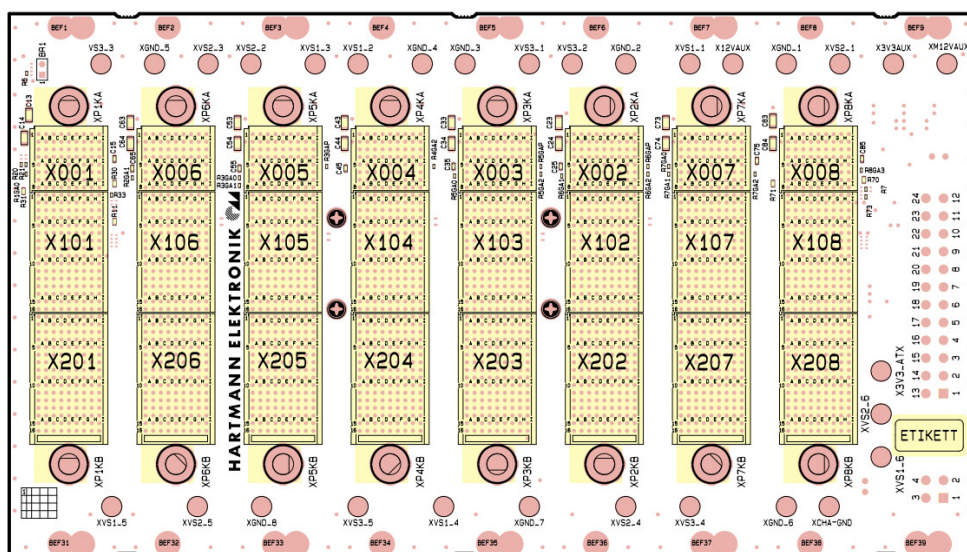
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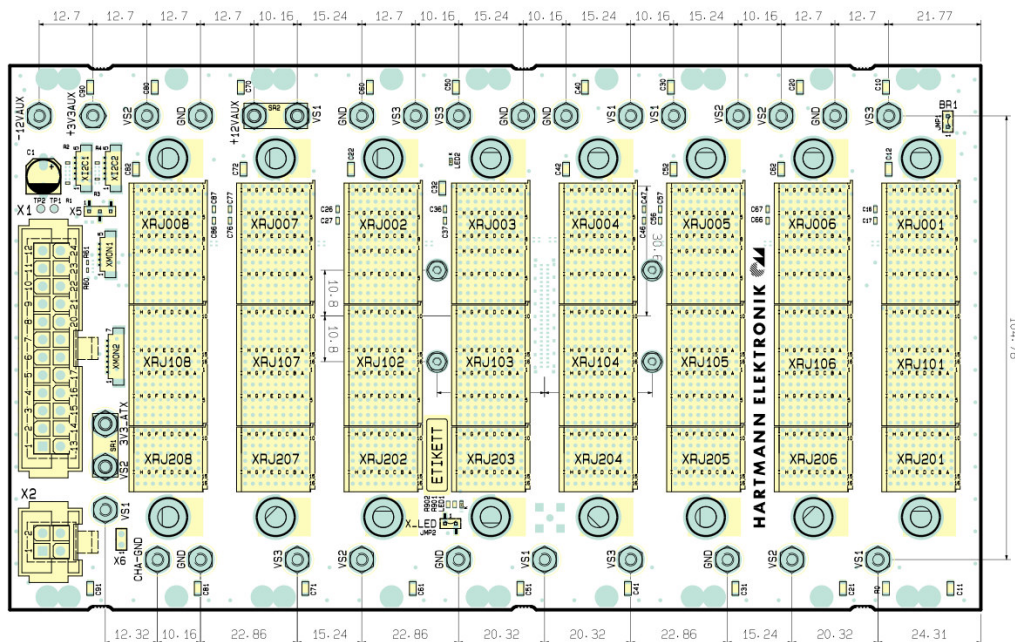


2) Drawings

Front side



Rear side



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3) Pin Assignment

Utility Plane Signals on P0

	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	No Pad*	Vs3	Vs3	Vs3
4	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1
6	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*
7	TCK	GND	TDO	TDI	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND

Utility Plane Signals on J0

	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Vs1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad*	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

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Payload Slot Profile SLT3-PAY-2F2U 14.2.3 — P1 & J1

Plug-in module P1				Row G	Row F	Row E		Row D	Row C	Row B		Row A
						Even	Odd			Even	Odd	
Bplane J1				Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	X8	x4 / 2x2 / 4x1	GDiscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2				GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3				P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4				GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Data Plane Port 2	X8	x4 / 2x2 / 4x1	SYS_CON*	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
6				GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
7				Reserved	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
8				GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
9	User Defined			UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10				GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11				UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12				GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13				UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14				GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15	Control Plane			Maskable Reset*	GND	GND-J1	CPutp02-TD-	CPutp02-TD+	GND	GND-J1	CPutp02-RD-	CPutp02-RD+
16				GND	CPutp01-TD-	CPutp01-TD+	GND-J1	GND	CPutp01-RD-	CPutp01-RD+	GND-J1	GND

Payload Slot Profile SLT3-PAY-2F2U 14.2.3 — P2 & J2

Universal Ground Pattern User Defined pins for J2 acc. Table 6.3.3.1-5

Backplane J2	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	UD	UD	UD	UD	UD	GND	UD	UD	UD
2	GND	UD	UD	GND	UD	UD	UD	UD	GND
3	UD	UD	UD	UD	UD	GND	UD	UD	UD
4	GND	UD	UD	GND	UD	UD	UD	UD	GND
5	UD	UD	UD	UD	UD	GND	UD	UD	UD
6	GND	UD	UD	GND	UD	UD	UD	UD	GND
7	UD	UD	UD	UD	UD	GND	UD	UD	UD
8	GND	UD	UD	GND	UD	UD	UD	UD	GND
9	UD	UD	UD	UD	UD	GND	UD	UD	UD
10	GND	UD	UD	GND	UD	UD	UD	UD	GND
11	UD	UD	UD	UD	UD	GND	UD	UD	UD
12	GND	UD	UD	GND	UD	UD	UD	UD	GND
13	UD	UD	UD	UD	UD	GND	UD	UD	UD
14	GND	UD	UD	GND	UD	UD	UD	UD	GND
15	UD	UD	UD	UD	UD	GND	UD	UD	UD
16	GND	UD	UD	GND	UD	UD	UD	UD	GND

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Switch Slot Profile SLT3-SWH-6F6U 14.4.1 — P1 & J1

Plug-In	Row G	Row F	Row E		Row D	Row C	Row B		Row A
Module P1			Even	Odd			Even	Odd	
Bplane J1	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	GDIscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2	GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3	P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4	GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	SYS_CON*	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
6	GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
7	Reserved	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
8	GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
9	UD	GND	GND-J1	DP03-TD0-	DP03-TD0+	GND	GND-J1	DP03-RD0-	DP03-RD0+
10	GND	DP03-TD1-	DP03-TD1+	GND-J1	GND	DP03-RD1-	DP03-RD1+	GND-J1	GND
11	UD	GND	GND-J1	DP03-TD2-	DP03-TD2+	GND	GND-J1	DP03-RD2-	DP03-RD2+
12	GND	DP03-TD3-	DP03-TD3+	GND-J1	GND	DP03-RD3-	DP03-RD3+	GND-J1	GND
13	UD	GND	GND-J1	DP04-TD0-	DP04-TD0+	GND	GND-J1	DP04-RD0-	DP04-RD0+
14	GND	DP04-TD1-	DP04-TD1+	GND-J1	GND	DP04-RD1-	DP04-RD1+	GND-J1	GND
15	Maskable Reset*	GND	GND-J1	DP04-TD2-	DP04-TD2+	GND	GND-J1	DP04-RD2-	DP04-RD2+
16	GND	DP04-TD3-	DP04-TD3+	GND-J1	GND	DP04-RD3-	DP04-RD3+	GND-J1	GND

Switch Slot Profile SLT3-SWH-6F6U 14.4.1 — P2 & J2

Plug-In	Row G	Row F	Row E		Row D	Row C	Row B		Row A
Module P2			Even	Odd			Even	Odd	
Bplane J2	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	UD	GND	GND-J2	DP05-TD0-	DP05-TD0+	GND	GND-J2	DP05-RD0-	DP05-RD0+
2	GND	DP05-TD1-	DP05-TD1+	GND-J2	GND	DP05-RD1-	DP05-RD1+	GND-J2	GND
3	UD	GND	GND-J2	DP05-TD2-	DP05-TD2+	GND	GND-J2	DP05-RD2-	DP05-RD2+
4	GND	DP05-TD3-	DP05-TD3+	GND-J2	GND	DP05-RD3-	DP05-RD3+	GND-J2	GND
5	UD	GND	GND-J2	DS01-TD0-	DS01-TD0+	GND	GND-J2	DS01-RD0-	DS01-RD0+
6	GND	DS01-TD1-	DS01-TD1+	GND-J2	GND	DS01-RD1-	DS01-RD1+	GND-J2	GND
7	UD	GND	GND-J2	DS01-TD2-	DS01-TD2+	GND	GND-J2	DS01-RD2-	DS01-RD2+
8	GND	DS01-TD3-	DS01-TD3+	GND-J2	GND	DS01-RD3-	DS06-RD3+	GND-J2	GND
9	UD	GND	GND-J2	CSutp01-TD-	CSutp01-TD+	GND	GND-J2	CSutp01-RD-	CSutp01-RD+
10	GND	CPutp05-TD-	CPutp05-TD+	GND-J2	GND	CPutp05-RD-	CPutp05-RD+	GND-J2	GND
11	UD	GND	GND-J2	CPutp04-TD-	CPutp04-TD+	GND	GND-J2	CPutp04-RD-	CPutp04-RD+
12	GND	CPutp03-TD-	CPutp03-TD+	GND-J2	GND	CPutp03-RD-	CPutp03-RD+	GND-J2	GND
13	UD	GND	GND-J2	CPutp02-TD-	CPutp02-TD+	GND	GND-J2	CPutp02-RD-	CPutp02-RD+
14	GND	CPutp01-TD-	CPutp01-TD+	GND-J2	GND	CPutp01-RD-	CPutp01-RD+	GND-J2	GND
15	UD	GND	GND-J2	UD	UD	GND	GND-J2	UD	UD
16	GND	UD	UD	GND-J2	GND	UD	UD	GND-J2	GND

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4) I2C connector

There are 2 connectors for system- management I2C1 and I2C2.

For customer specific board assembly are Zero-Ohm resistors available.

Usable voltages for I2C are 3.3V-AUX

I2C1

1	I2C1_SCL
2	GND
3	I2C1_SDA
4	I2C1_PWR
5	NC

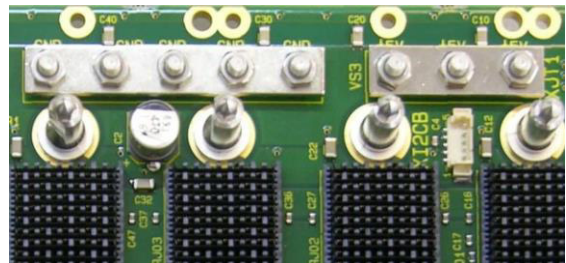
I2C2

1	I2C2_SCL
2	GND
3	I2C2_SDA
4	I2C2_PWR
5	NC

5) Power Studs M3

The main operating voltages (+12V, +3.3V, +5V) and GND are supplied with M3 screw terminals. The auxiliary operating voltages are supplied via M3 screw terminals.

Optimal daughter board supply and trouble-free operation are ensured by the arrangement of the feed modules on the backplane.



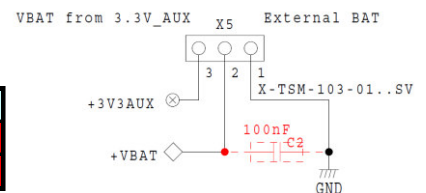
6) VBAT X5

Normally a battery voltage with approximately 3V is available at Pin VBAT of connector VPX-J1.

The voltage is externally accessible with connector X5 or internally using 3.3V_AUX by closing Jumper BR2.

VBAT X5

1	GND
2	+VBAT
2	+3.3V_AUX



7) NVMRO

If Jumper BR1 is closed NVRMO is set to memory writeable.

BR1

1	NVMRO
2	GND

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8) Power connection (ATX, ATX4 and M3 screw):

The main operating voltages and GND are supplied with M3 screw terminals or connector X1 (fits to ATX connector without locking mechanism). The auxiliary operating voltages are supplied via M3 screw terminals. Optimal daughter board supply and trouble-free operation are ensured by the arrangement of the feed modules on the backplane.



XATX4	Signal
1	GND
2	GND
3	+12V
4	+12V

XATX	Signal	Signal	XATX
1	+3.3V	+3.3V	13
2	+3.3V	-12V	14
3	GND	GND	15
4	+5V	PS_ON	16
5	GND	GND	17
6	+5V	GND	18
7	GND	GND	19
8	PWR_OK	Res	20
9	+5VSB	+5V	21
10	+12V	+5V	22
11	+12V	+5V	23
12	+3.3V	GND	24



If Jumper X6 is closed ATX power supply starts automatically.

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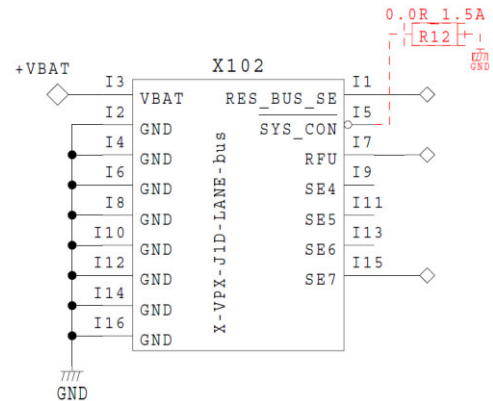


9) SYSCON

By setting the signal Syscon to GND the system slot is defined.

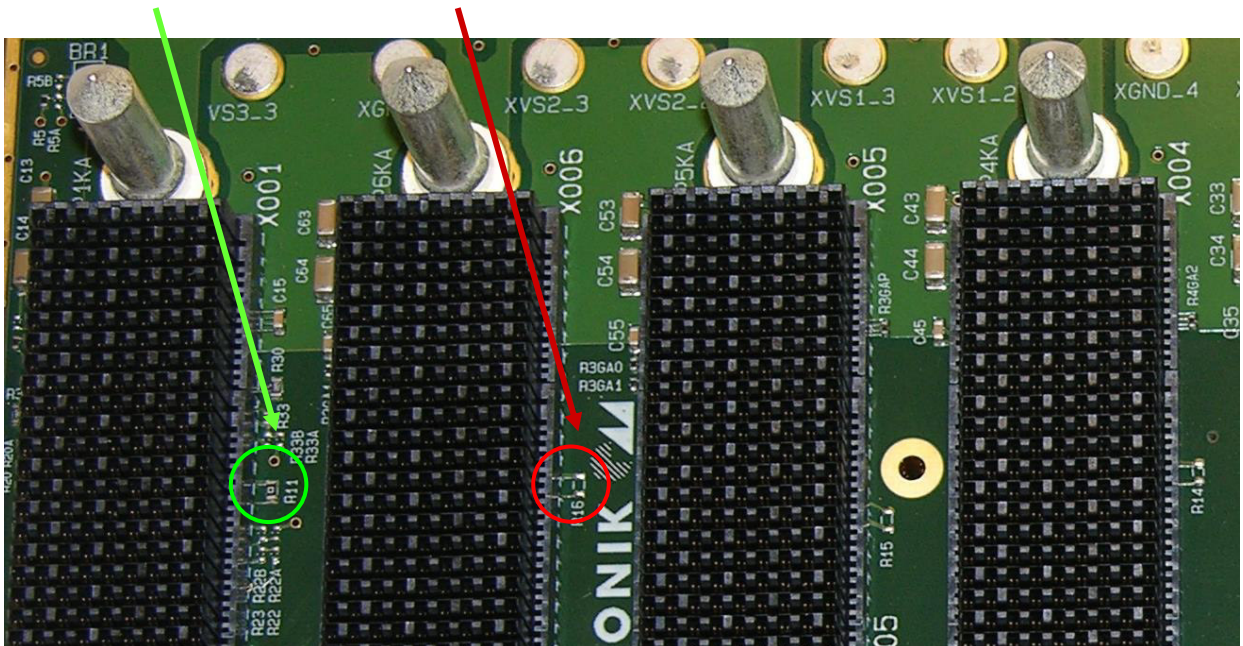
The system slot position is changeable by dislocating the 0 Ohm resistor R11, ... R12 by Hartmann Electronic.

In general the system slot is slot 1.



connected

not connected



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